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TUTORIAL TOPIC:

Compact Modeling of Semiconductor Devices

TUTORIAL:

In the first part of the tutorial compact modeling of bipolar devices will be elaborated. Starting from the p-n junction diode, we will discuss on how to obtain an equivalent circuit model for an n-p-n transistor. Key model equations will be elaborately discussed from the viewpoint of modern silicon germanium heterojunction bipolar transistors. Extraction of the model parameters and Verilog-A implementation of the model will be elaborated. Few research problems and their possible solutions on the non-quasi-static delay and correlated noise models will be presented. A discussion on the compact model development of high voltage LDMOS transistor will follow.

In the second part, we will discuss on compact modeling of MOS transistors. We will start with threshold voltage based industry standard bulk MOSFET models BSIM3/4 and then discuss charge based BSIM6 model. Symmetry in MOS models and its impact on harmonic balance simulation will be explained. Then will move on to limitations of bulk MOSFET and introduce multigate transistors FinFET and UTBSOI FET. Here will talk about industry standard multigate models for FinFET and nanowire transsitros. Finally, we will close with discussion on future of FinFET with III-V and Ge MOSFET.

PROFILE:

Anjan Chakravorty received his B. Tech., M. Tech., and Ph.D. degree from University of Kalyani, University of Calcutta, and Indian Institute of Technology Kharagpur, in 1999, 2001, and 2005, respectively. He worked as a guest scientist in modeling group at Innovations for High Performance Microelectronics, IHP GmbH, Germany for nine months in between 2003 and 2004. From 2005 to 2006, he was a Post-Doctoral Fellow at Dresden University of Technology, Germany, where he worked on bipolar transistor compact model, HICUM. From 2007 onwards he is with the Department of Electrical Engineering, IIT Madras where he is presently working as an Associate Professor. His research interests include compact modeling of microelectronic devices, on-chip inductor design, and computational

electronics.

Yogesh Singh Chauhan is an assistant professor in department of Electrical Engineering at Indian Institute of Technology Kanpur, India. He received Ph.D. degree in compact modeling of high voltage MOSFETs in 2007 from EPFL Switzerland. During 2007-2010, he was manager in IBM Bangalore, where, he led compact modeling teams focusing on RF bulk and SOI transistors and ESD devices. During 2010-2012, he was postdoctoral fellow at University of California Berkeley, where he worked on development of bulk and multigate transistor models including BSIM6, BSIM-IMG and BSIM-CMG. He received IBM faculty award in 2013 for his contribution in compact modeling. He has co-authored over 50 conference and journal publications in the field of device compact modeling.