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TOPIC:

Quantum Well Heterostructures for Electronics and Photonics

ABSTRACT:

In this talk future semiconductor quantum well heterostructure devices for logic, memory and photonic interconnects will be discussed.

Future Si CMOS scaling for logic and memory is reaching practical and fundamental limits. To go beyond these limits novel materials like Ge, GeSn and III-Vs, together with innovative quantum well heterostructure devices are being aggressively studied. Heterogeneous integration of these materials on Si with novel device structures can take us to sub-10 nm regime. However there are many daunting problems to be solved before any of these technologies can be implemented. Most of these materials have low bandgap resulting in excessive leakage, especially band-to-band tunneling. Use of quantum-well heterostructures with wide-low-wide bandgaps where carrier transport takes place in a high mobility (low bandgap) material but high E-field occurs in the wide bandgap material can make it possible to reduce the leakage without sacrificing the transistor performance. Similarly, scaling of conventional 1-transistor 1-capacitor DRAM scaling has become problematic. A wide-low-wide bandgap MOSFET can be used to make a capacitorless 1-transistor DRAM, where the charge representing the state of the memory is stored in the low bandgap channel and is kept from leaking by the wide bandgap material source/drain, giving long retention time even for nanoscale devices. These techniques will allow us to scale to below 10 nm node.

With Cu/low-k interconnects also running into scalability problems, on- and off-chip optical interconnects will be required to meet the requirements of low latency,low power consumption and high bandwidth. Missing link in developing this is an on-chip laser. Ge is a strong candidate for this as although it is an indirect bandgap material, strain can be used to make it a direct bandgap material. Efficient light emission also requires a double heterostructure and conventionally is achieved by using different III-V materials. By varying strain in a Ge nanowire a wide-low-wide bandgap has been demonstrated in a single material and can be used for efficient light emission.

In nanoscale devices, especially in new materials, contact resistance (Rc), is becoming a limiting factor.

Unlike Si heavy doping is not practical in many of these materials to reduce Schottky barrier (\cdot B) height to minimize Rc. In metal/semiconductor (M/S) contacts Fermi level is pinned at the charge neutrality level ECNL due to metal-induced gap states (MIGS) caused by the penetration of wave functions of metal electrons into the semiconductor. This results in fixed M/S \cdot B irrespective of metal workfunction. One method to solve this problem is to modulate \cdot B by inserting an ultrathin metal oxide at the M/S interface to attenuate the metal electron wavefunction resulting in fewer MIGS thus depinning the Fermi level. This method has been demonstrated to reduce \cdot B and thus contact resistance in Si, Ge, GeSn and various III-Vs.

PROFILE:

Krishna Saraswat is Rickey/Nielsen Chair Professor of Electrical Engineering at Stanford University. He received Ph.D. from Stanford University in 1974 and B.E. from BITS, Pilani in 1968. He His research interests are in new and innovative materials, structures, and process technology of silicon, germanium and III-V devices and metal and optical interconnects for nanoelectronics, and high efficiency and low cost solar cells. He has supervised more than 80 doctoral students, 25 post doctoral scholars and has authored or co-authored over 740 technical papers. He is a Life Fellow of the IEEE. He received the Thomas Callinan Award from The Electrochemical Society in 2000, the 2004 IEEE Andrew Grove, Inventor Recognition Award from MARCO/FCRP in 2007, the Technovisionary Award from the India Semiconductor Association in 2007 and the Semiconductor Industry Association Researcher of the Year Award in 2012. He is listed by ISI as one of the 250 Highly Cited Authors in his field.