Prof. Subho Dasgupta
Institute of Nanotechnology (INT),
Karlsruhe Institute of Technology (KIT),
Hermann-von-Helmholtz Platz 1,
76344 Eggenstein-Leopoldshafen,
Germany.

TOPIC:

Printed and low-temperature processed oxide electronics

ABSTRACT:

Printed logics encompass a large fraction of activities in the field of printed electronics and therefore attracting increasing attention in recent years. While traditionally organic field-effect transistors (OFETs) were studied, solution-processed FETs from inorganic materials (mostly involving inexpensive and non-toxic metal oxides) have also been introduced relatively recently. Although, oxide semiconductors demonstrate by far superior electronic transport compared to the organic counterparts, however, for solution processed oxide electronics, there are still several challenges to overcome. Typically, two distinct ways for printing FET's from oxide semiconductors are considered. When devices are prepared from metal oxide precursors satisfactory performance has only been achieved for technically unacceptable process temperatures, which is beyond the glass transition temperature of commonly used, inexpensive (polymer, cellulose) substrates. Conversely, devices made from oxide nanoparticles suffer from ineffective gating due to the large interface roughness between the nanoparticulate film and the gate insulator.

In contrast to above approaches, a novel concept involving electrolyte gating will be presented that can overcome some of the above mentioned shortcomings. Electrolyte gating approach can offer semiconductor-dielectric conformal interface to any printed layer morphology and surface roughness; can also provide environmentally-stable and low voltage driven high performance devices. Furthermore, following this concept it is possible, for the first time, to fabricate completely room temperature processed oxide electronics, while at the same time demonstrating one order of magnitude superior device mobility compared to the printed OFETs. In addition, it will be shown that the speed of the electrolyte-gated FETs may not be limited by the ionic conductivity of the composite solid polymer electrolytes (CSPE) used in our study, it is rather the printing resolution that determines the channel length and alongside the maximum attainable switching speed.

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PROFILE:

Dr. Subho Dasgupta, a gold medalist from IIT Kharagpur, received his Ph. D. degree in Material Science from Technical University of Darmstadt (TUD), Germany in 2009, with 'Summa Cum Laude' the highest grade given for an outstanding PhD thesis. He is principle investigator (topic: printed electronics) and research group leader at Institute of Nanotechnology (INT), Karlsruhe Institute of Technology (KIT), Germany, since 2012. In 2013/14 he has also worked as a visiting scientist at Lawrence Livermore National Laboratory, USA. His research interest includes printed electronics, nanomagnetism, electrochemistry, Li-ion batteries, 3-dimensional monolithic graphene etc. He has authored/co-authored 22 research articles, and filed 8 patent applications which are either granted or under review.