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TOPIC:

Low temperature, low pressure Cu-Cu bonding for 3-D IC integration

ABSTRACT:

The demand for more functionality within a single chip is growing in every decade. To be on track of Moore's law the viable option was aggressive scaling down of the device dimensions. As the device dimensions have already reached to its fundamental limit scaling down of dimension is no longer a reasonable choice. Paradigm shift is in architecture necessary to satisfy the ever-growing demand of higher performance. 3 Dimensional Integration can bring such possibility in reality. 3D Integration is advantageous over conventional planer integration in many ways like (1) higher bandwidth (2) smaller foot print (3) heterogeneous integration (4) shorter interconnect. Copper is the best choice for electrical interconnect between the two staked wafer. Thermo compression technique is the dominant method for creating interconnects. These have to achieve at low temperature and low pressure bonding for reliability of ICs. However the oxidation of cu surface is the key bottleneck to achieve low temperature low pressure bonding. In this talk we discuss the process to protect Copper from oxidation. Also other novel method has been developed to achieve low temperature low pressure bonding.

PROFILE:

Shiv Govind Singh is an associate professor in Indian Institute of Technology (IIT) Hyderabad. He had been a visiting faculty in Purdue University and IIT Bombay. He received his PhD degree from IIT Bombay and had done his post doc from Nanyang Technological University, Singapore from 2008 to 2009. He has more than 75 peer reviewed papers included journals, conference, paten and book chapters. His interests include 3-D ICs, bio-sensors, lab on chip, energy harvesting circuit and RF MEMS.