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TOPIC:

Technology - Design interaction: Lessons from the CMOS world

ABSTRACT:

Continuous scaling of MOS devices has been the foundation of the digital revolution for the last four decades. Classic lithography based device scaling stopped at the 130nm node. Improvement in power-performance is now achieved by innovations in materials and device architectures. But it has created new set of problems which demanded closer working for circuit designers and process/device engineers. The demand of circuit designers can impact the selection of solutions for the device step-up plan and similarly lack of technology options can put constraints in design styles. In this talk i will discuss the lessons learnt during CMOS technology development through some examples which could be useful in making informed choices in the world of emerging devices.

PROFILE:

Deleep R. Nair did his B.Tech in Electronics and Communication Engg at Regional Engineering College Calicut (now NIT Calicut), M.Tech and PhD at IIT Bombay. He then worked close to 7 years at IBM Semiconductor Research and Development Center, East Fishkill, NY on advanced logic technology development. He has been working as an Assistant Professor in the Department of Electrical Engg, IIT Madras for the last 2 years.