CeNSE Newsletter

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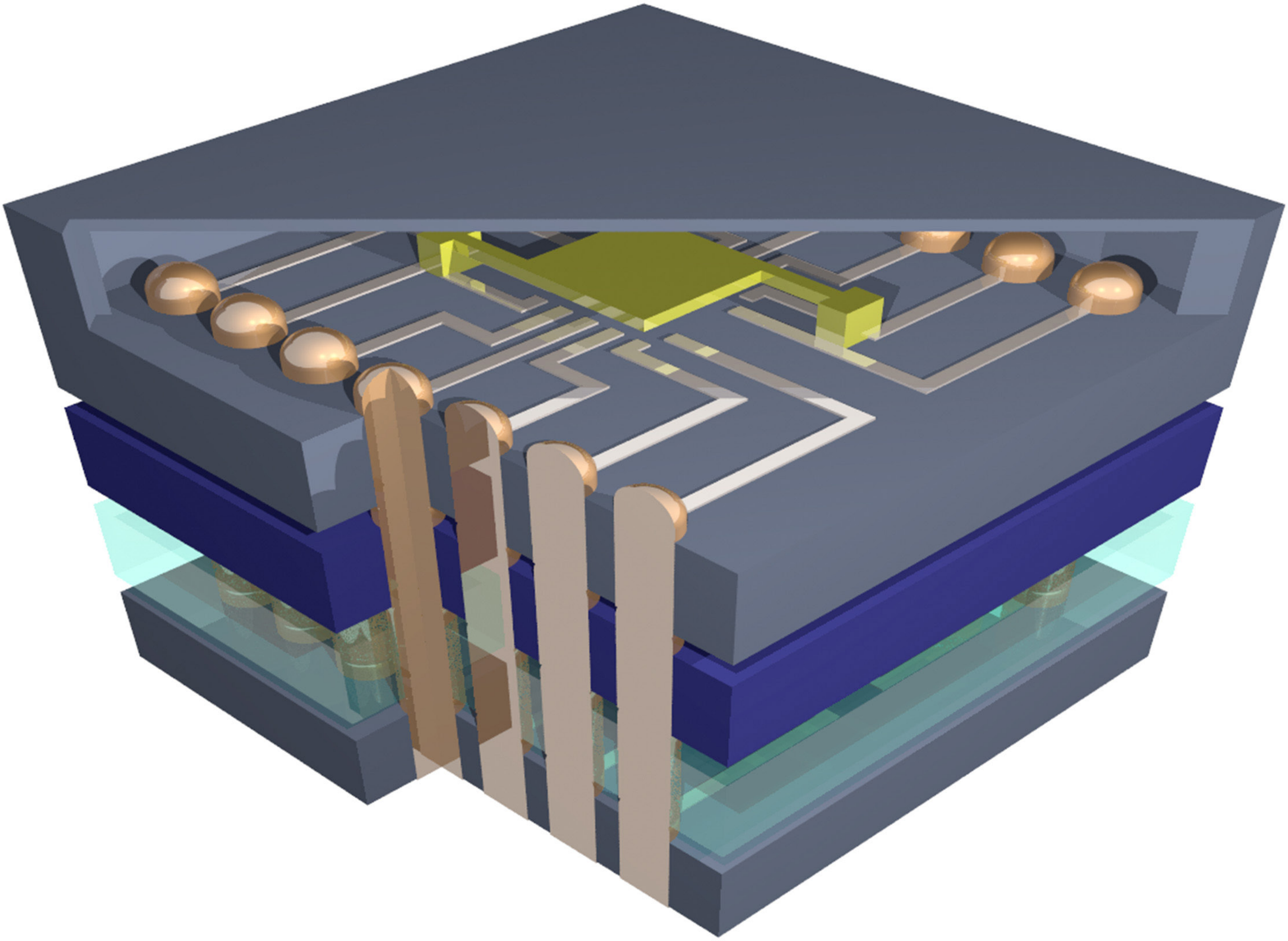


CONTENTS

Cover photo: A multi-sensor 3D-integrated heterogeneous micro-nano-system

NPMASS- Exhibition on 22nd August 2015 at IISc

Vijayaraju

About NPMASS

The National Programme on Micro and Smart Systems (NPMASS) was sanctioned by the Government in September 2007 with a budget of Rs 195 Crores. The Programme will close in Dec 2015. It is a joint programme of five scientific departments of the Government, namely, DRDO, DoS, DST, DeitY and CSIR. The programme is being executed through the Aeronautical Development Agency, Bangalore.

The main objective of the NPMASS is realization of products/devices/ subsystems based on MEMS and Smart Materials Technology, and their field demonstration. Various developments were undertaken to support applications in aerospace and defense areas, and to achieve commercial exploitation in various sectors such as automotive, biomedical, environmental safety and food technology. Health-monitoring of infrastructure in the civilian sector was also attempted. Various infrastructural facilities were also established, such as component and system level characterization facilities, LTCC packaging, and polymer micro-fabrication.

About the Event

An exhibition was organized to showcase the achievements of NPMASS - both devices and technologies developed under the programme - to the scientists and engineers of DRDO and other Government departments. This Display-cum-Demonstration exhibition was held on 22nd August 2015 in IISc at CeNSE and the Department of Aerospace Engineering.

About 50 scientists from DRDO Labs and other Government departments attended the exhibition. About 40 devices and technologies developed under NPMASS were demonstrated by Project teams led by the Chairmen of various Project Committees driving the NPMASS programme. A compendium with details of all the projects under NPMASS was compiled for this occasion and distributed to all the participants.

Details of Demonstrations

The devices and technologies demonstrated are listed below:

->MEMS sensor systems: Pressure sensors, Accelerometers, Gyroscopes, RF devices & Gas sensors

->Smart materials: SMA wires, including high-temperature wires, Piezo films and coatings and PZT actuators

->Smart material-based aircraft applications: Adaptive trailing edge deflection control, de-icing, engine mount vibration control, SMA-based trim tab and aerofoil morphing

->Structural Health monitoring: Rapid online NDE technologies for aircraft, Wireless motes for civil infrastructure monitoring

->Integrated Vehicle Health Monitoring technology initiatives in aircraft and automotive sub-systems

->Bio-Medical applications: Diagnostic systems for cardiac markers, uro-pathogesn, lipid profile, explosives, retinoblastoma, marine food health; Drug delivery system elements – Micro pumps, Needles and control system

->Software: Modelling micro- and nano-systems (CONE); Software architecture for Rapid SHM for aircraft maintenance; Aircraft IVHM s/w framework

Response

Dr. K. Tamilmani, DS & DG (Aero), Dr. Satish Kumar, DS, DG (MSS) & CC R&D (TM & SAM) and Dr. K.D. Nayak, DS & DG (MED & CoS & CS) were among the invitees who visited the exhibition stalls and appreciated the efforts of Project Teams. The delegates interacted actively with the project teams, and discussed applicability and use of the technologies developed for their platforms, including aspects such as specifications, technology behind the devices, status of development, and possible improvements for their eventual use.

During the concluding session, the distinguished invitees from DRDO appreciated the technologies and devices developed under the Programme. They emphasized that all these should reach the actual users in DRDO and be implemented on relevant platforms. Dr Aatre, former SA to RM, Secretary, Defence R&D, and presently Chairman B-SMART (NPMASS), emphasised that active participation from users and industries is essential to take these technologies and devices into the user domain, and hoped that this would happen soon. Dr Vijayaraju, PD (NPMASS), thanked all the invitees and the project teams for participating in this exhibition and making it a success.

SYSTEM SCALING

Thinking Beyond the Chip

Prosenjit Sen

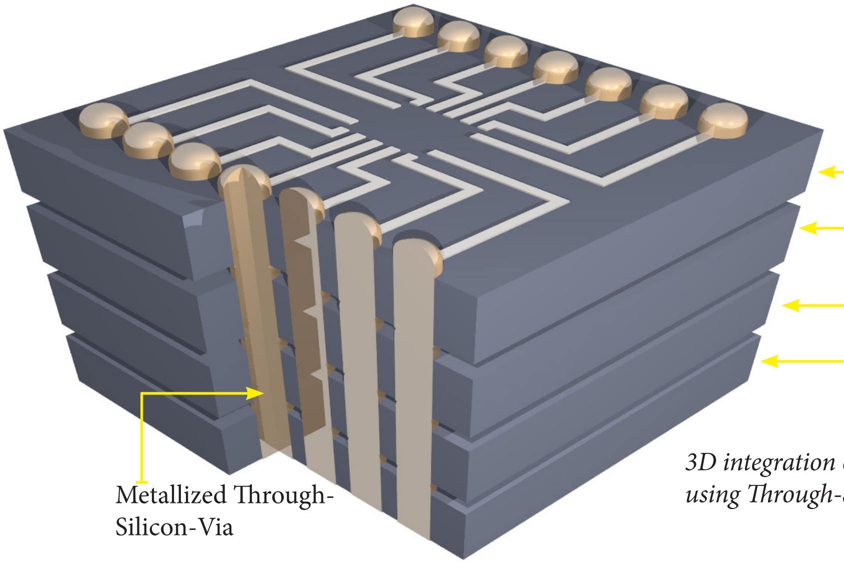
In the past decades, the semiconductor industry has invested significant efforts into providing increased functionality in smaller chips through continuous shrinking of the critical dimensions of the transistor. The critical dimension in the latest Intel microprocessors is close to 14 nm, which is approximately 60 silicon atoms-wide. With critical dimensions reaching fundamental limits, the community is looking towards 3D integration for enhancement of functionality in a given volume of silicon. In this technology, various dies, often of similar functionality and design (e.g., memory), are thinned down to tens of micrometers, and assembled using various wafer-level bonding technologies. Metallized through-silicon-vias (TSV), as shown in the figure, are used to make electrical connection between the different integrated circuits (IC) in the stack.

In traditional printed circuit board (PCB)-based assembly, the limited number of pins in chip packages and the larger critical dimensions on PCBs often restrict the communication bandwidth between chips. As chip-to-chip communication speeds are increasing, driving the larger and longer interconnects on PCBs is leading to a considerable amount of power expended on communication. In comparison, 3D integration of IC's not only leads to smaller system volumes but also allows high density parallel connections between the chips. 3D integration also leads to significantly shorter interconnect lengths. These benefits allow for a significantly higher bandwidth between chips, at lower power consumption.

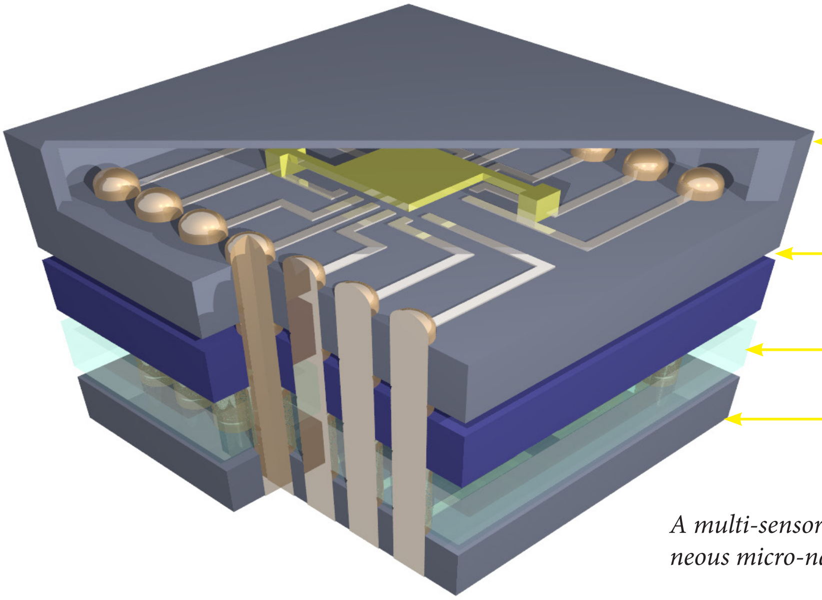
To maximize profits by increasing the number of devices in a wafer, the MEMS industry is also working hard towards reducing device footprint through innovations in design and processing technology. In several cases, miniaturization of MEMS devices is currently limited by various processing capabilities. For example, reduction in footprint of inertial sensors, while maintaining their minimum detection limits (which depends on weight of proof mass, requires improvement in the maximum aspect ratio achievable in deep reactive-ion etching. Although this approach of miniaturization is leading to reduction in the sizes of the individual devices, conventional packaging approach during integration with IC's and other electronics leads to systems with much larger dimensions.

The relatively large sizes of MEMS-based systems have not been an issue so far due to the limited number of these devices used in any application, and the availability of large batteries to power such bulky systems. However, with the advent of the Internet of Things (IoT), it has been envisaged that almost everything that we interact with will become smart through integrated sensors and actuators. The data captured by the sensors will be available over the internet for decision making. Several leading agencies have predicted that, in the near future, there will be approximately 1000 such sensor nodes per person capturing and uploading a variety of information. Such a large number of sensor nodes per person would only be possible through miniaturization of the sensor systems which require minimal energy.

Such sensor systems will incorporate multiple different sensors (fabricated using different technologies on different substrates) to be closely integrated with a microcontroller, communication chip (often wireless), and an energy source. Through reduction/elimination of traditional packaging and PCB-based integration schemes, we can develop a truly micro-nano-system. Such self-powered micro-nano sensor nodes can be independently



3D integration of Semiconductor IC using Through-Silicon-Via Technology



A multi-sensor 3D-integrated heterogeneous micro-nano-system

deployed to collect and transmit information. For example, a multiple of such nodes can be deployed to monitor the health of structures such as a bridge. As a vehicle passes over the bridge, these nodes would harvest energy from the ambient vibration. The harvested energy will be used to make measurements on the structural integrity of the bridge and transmit them to a neighbouring data hub. Similar nodes with different sensors can be used to monitor pollution, traffic, etc. Realizing micro-nano systems will require a collaborative interdisciplinary R&D effort encompassing various fields. Such efforts have been initiated at CeNSE, as we recognize the field to be evolving and realize that we, as a country, have a great opportunity to make international impact.

View faculty profile:
www.cense.iisc.ernet.in/people/faculty/prosen.htm

Micromachined Accelerometers with Mechanical Amplification

What does it take to design, fabricate, characterize, package, test, and calibrate a microelectromechanical systems (MEMS) device in an academic setting? Well, we first need a problem and then some thought to address that problem creatively. There is neither a dearth of problems nor of ingenious approaches to solve them. What we need beyond these are facilities to fabricate, characterize, package, test, and calibrate the MEMS devices we conceive and design. Today, CeNSE has all these. The necessary conditions exist now. Are they sufficient? No. Two things make for "sufficient": an able and dedicated student and conditional financial support.

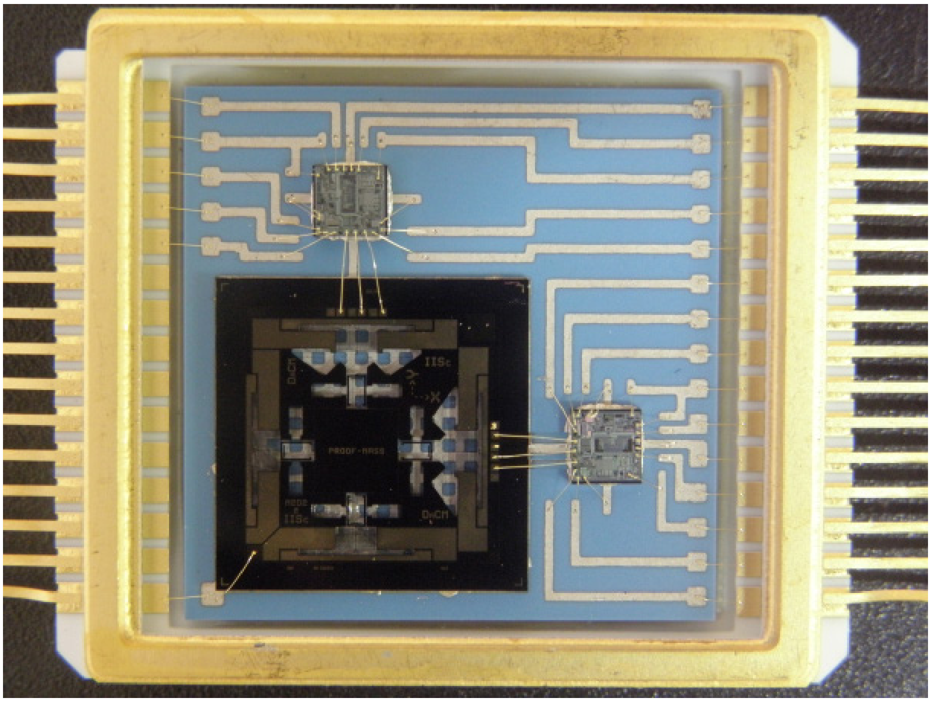
I want to tell you briefly about how we developed an accelerometer from start to finish, i.e., from a flash of an idea all the way to the packaged device, a few years before CeNSE was set up, i.e., before necessary conditions were met. Our effort culminated when the CeNSE building took shape and the accelerometer devices were one of the first fruits of labour at CeNSE; they were tested in the Characterization lab. What did I have to do it? I had Sambuddha Khan as my PhD student, co-advised by Prof. H. S. Jamadagni of DESE. And I had the unflinching funding support from Dr. V. Natarajan of NPOL, Kochi, in the form of three phases of CARS projects.

We wanted to develop micromachined accelerometers with high resolution. High resolution needs excellent sensitivity (measured in V/g, i.e., how much output voltage do you get per unit gravitational acceleration?) and low noise-floor (measured in g/rootHz, i.e., how much equivalent acceleration is there due to noise sources over a range of frequencies?). High-resolution accelerometers are expensive, unlike the day-to-day ones used in mobile phones, cars, and toys. Our original idea to attain high resolution was simple and it turned out to be effective.

It may surprise many to learn that noise in a mechanical sensing element is about an order of magnitude lower than the noise in electronic elements. So, in an electromechanical device, it makes more sense to amplify the signal mechanically rather than electronically. This is because noise too gets amplified, along with the signal. So, we started to focus on mechanical amplification. Electronics people may please note that mechanical amplification is not like an op-amp wherein additional power is used for amplification. Our mechanical amplifier is more like a transformer or a lever: it transforms high force and small displacement at its input to large displacement and low force. This principle is perfect for a capacitive accelerometer, which uses the differential displacement between electrostatic comb-fingers to sense acceleration.

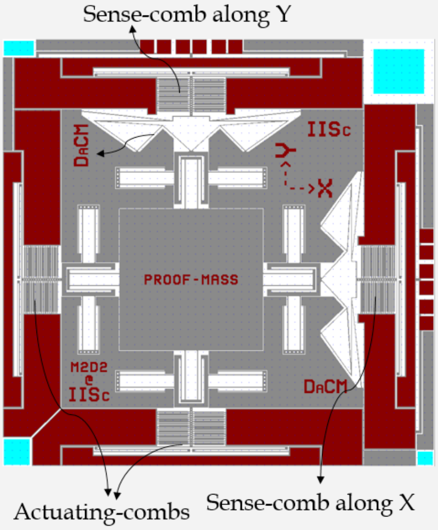
The design challenge ahead of Sambuddha was clear: increase the output displacement at the sensing combs through a mechanical amplifier, without taking up additional space on the wafer. That is, cut into the proof-mass area and use it for amplification. The work of former students, Prof. Girish Krishnan (UIUC, USA, then an MSc(Eng.) student in my group) and Dr. Sudarshan Hegde (now with Bosch-Bengaluru in the Automotive Electronics division) had laid the foundation. We had mechanical amplifiers that we had christened "Displacement-amplifying Compliant Mechanisms" or DaCMs for short. Sambuddha meticulously designed them; got them made at an SOI-MUMPS foundry and later at ECS Partners, a spinoff from the University of Southampton, UK; went from pillar to post for electronic integration and packaging and got help from CMET-Pune and SI Microsystems-Bengaluru; had ups and downs, and finally got them all working. He had single-axis, dual-axis, and tri-axis accelerometers done, and took them to at least TRL 6.

G. K. Ananthasuresh



The innards of a packaged dual-axis accelerometers. DaCMs are marked on the wafer.

Dual-Axis Accelerometer with DaCMs



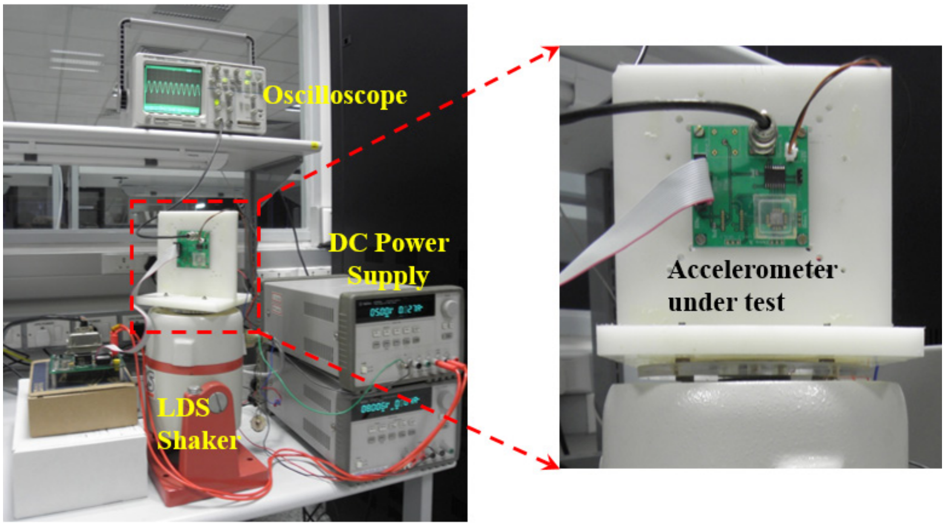
LUMPED PARAMETERS OF THE ACCELEROMETER

Parameters	Values
Suspension stiffness (k_z) and mass (m_z) of the actuation side	23 N/m and 0.58×10^{-6} kg
Stiffness of the external suspensions (k_{ext}) and mass of the sense-comb (m_{ext})	0.08 N/m and 0.0155×10^{-6} kg
k_{ci} and k_{co} values of the DaCM	24.14 N/m and 32.32 N/m
m_{ci} and m_{co} values of the DaCM	4.98×10^{-8} kg and 5.35×10^{-10} kg
Mechanical Advantage (n) of the DaCM	-6.44

PERFORMANCE SPECIFICATIONS OF THE ACCELEROMETER

Specifications	Analytically estimated	FE Simulated
Static displacement sensitivity	0.594 μm/g	0.586 μm/g
First two in-plane modal frequencies (without damping)	1007.5 Hz (both axes)	1030.56 Hz (both axes)
Net Amplification (NA)	1.56	1.53

Mask layout of the dual-axis accelerometer

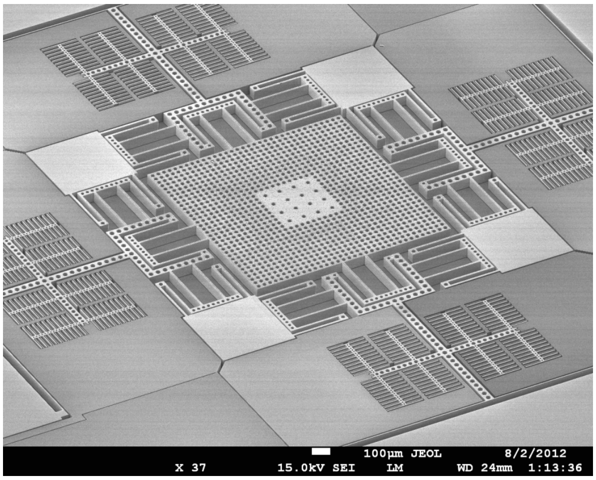


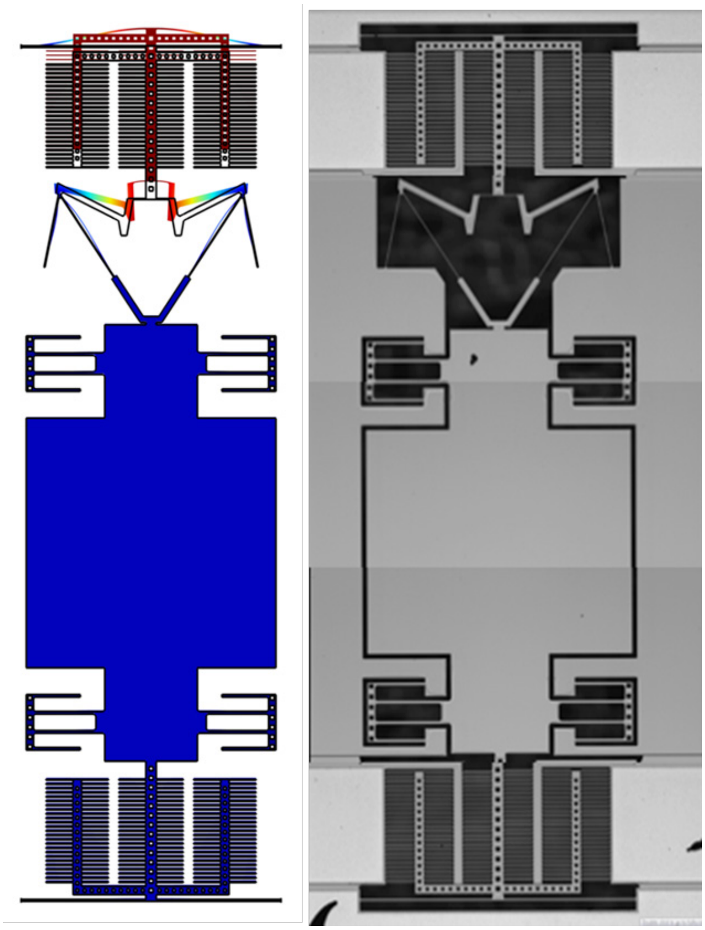
Testing in the CeNSE characterization facility

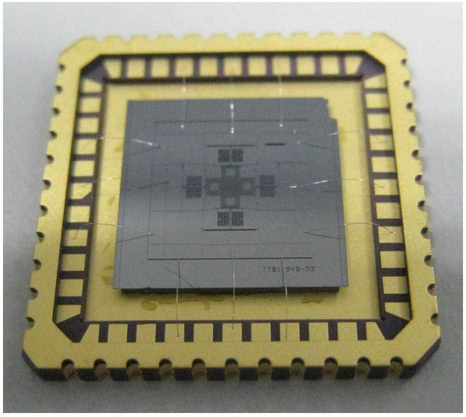
Right: SEM image of the tri-axial accelerometer

Below: Single-axis accelerometers: finite element simulation that shows amplification at the sensing combs and fabricated silicon device.

Bottom: Packaged tri-axial accelerometer with partial packaging







A pleasant surprise in this work was that one did not have to sacrifice bandwidth for high resolution or vice versa. Mechanical amplification helps one achieve both in one design. The bottom line: there are rewards to reap when one focuses on mechanical design. A DaCM, which is a glorified lever, can work wonders in the micro world. Archimedes, who had said that "give me a lever and I will tilt the whole earth", would have been pleased if he had known this.

View faculty profile:
www.mecheng.iisc.ernet.in/~suresh

Further Reading:

1. Khan, S. and Ananthasuresh, G. K., "Improving the Sensitivity and Bandwidth of In-plane Capacitive Micro-accelerometers using Compliant Mechanical Amplifiers," IEEE Journal of Microelectromechanical Systems, 23(4), 2014, pp. 871-887.

2. Khan S. and Ananthasuresh, G. K., "A Micromachined Wideband In-plane Single-axis Capacitive Accelerometer with a Displacement-amplifying Compliant Mechanism," Mechanics-based design of Structures and Machines, Vol. 42(3), 2014, pp. 355-370.

3. Krishnan, G., Kshirasagar, C.U., Bhat, N., and Ananthasuresh, G.K., "Micromachined High-Resolution Accelerometers," The Journal of the Indian Institute of Science: A Multidisciplinary Reviews Journal, Vol. 87 (3), 2007, pp. 333-362.

Deep Reactive Ion Etching (DRIE) Capability at CeNSE

Sunanda Babu

The National Nanofabrication Centre (NNfC) at CeNSE is a CMOS/MEMS/NEMS – capable research facility located at IISc. The Centre houses state-of-the-art research equipment for both fabrication and in-line characterization of the devices.

At NNfC, various unit processes are being developed and optimised by tapping into the capabilities of the various processing tools and integrated into CMOS/MEMS/NEMS/Photonics prototypes. DRIE or Deep Reactive Ion Etching, an attractive MEMS solution, is one of the offerings on the platter of unit processes.

Deep reactive-ion etching (DRIE) is a highly anisotropic etch process used to create deep high aspect ratio holes or trenches in wafers/substrates; predominantly in silicon. It was primarily developed for microelectromechanical systems (MEMS) devices that require deep-Si etch. In this process, etch depths of greater than 100 µm can be achieved with almost vertical sidewalls. Traditional dry etch schemes are designed for thin film patterning. But with respect to building high aspect ratio micromachines and nanomachines through dry etching, three major limitations had to be overcome, a) low Si etch rates, b) inability to maintain high anisotropy over etch depths >10 µm c) poor protection performance of masking layers for long etches.

DRIE is considered an attractive solution to address these limitations. The primary technology is based on the "Bosch Process" (patented by Robert Bosch GmbH, Stuttgart, Germany), wherein two different gas compositions are alternated in the reactor. The first gas composition creates a polymer on the surface of the substrate, and the second gas composition etches the substrate. The polymer is immediately sputtered away by the physical part of the etching, but only on the horizontal surfaces and not the sidewalls. Since the polymer only dissolves very slowly in the chemical part of the etching, it builds up on the sidewalls and protects them from etching. As a result, etching aspect ratios of 50 to 1 can be achieved.

The STS LpX Pegasus is the DRIE tool available at NNfC. It can process 4" wafers or smaller samples. We have HF- and LF-based processes (based on the Bosch process) with etch rates varying from 4 µm /min to 30 µm min and scallop size ranging from 12nm to 1.2 µm, as shown in figure 1.

The tool has recipes that control chamber pressure, gas flows (SF_6, C_4F_8, O_2, Ar), platen temperature (-20ºC to 40ºC), coil power (3000 W), platen power, and dep/etch times. Only silicon, photoresist, silicon nitride (Si_3N_4) and SiO_2 are allowed in the chamber. Metal-containing samples are not allowed in the tool. One of the issues with DRIE process is the inherent sidewall roughness or "scallops" made during etching. By optimizing the process, a smooth profile can be achieved, as shown in figure 2.

Superhydrophobic surfaces have become very popular in recent years due to their extreme water repellence. Simple applications are: non-stick surfaces, friction reduction for speed boats etc. To name a few other applications, such nanostructured surfaces are also used as a low reflectivity surfaces, anti-bacterial surfaces, bio-sensors, piezo-electric nano generators and in renewable energy applications. DRIE process optimisation has been done in our facility to

Fig 1

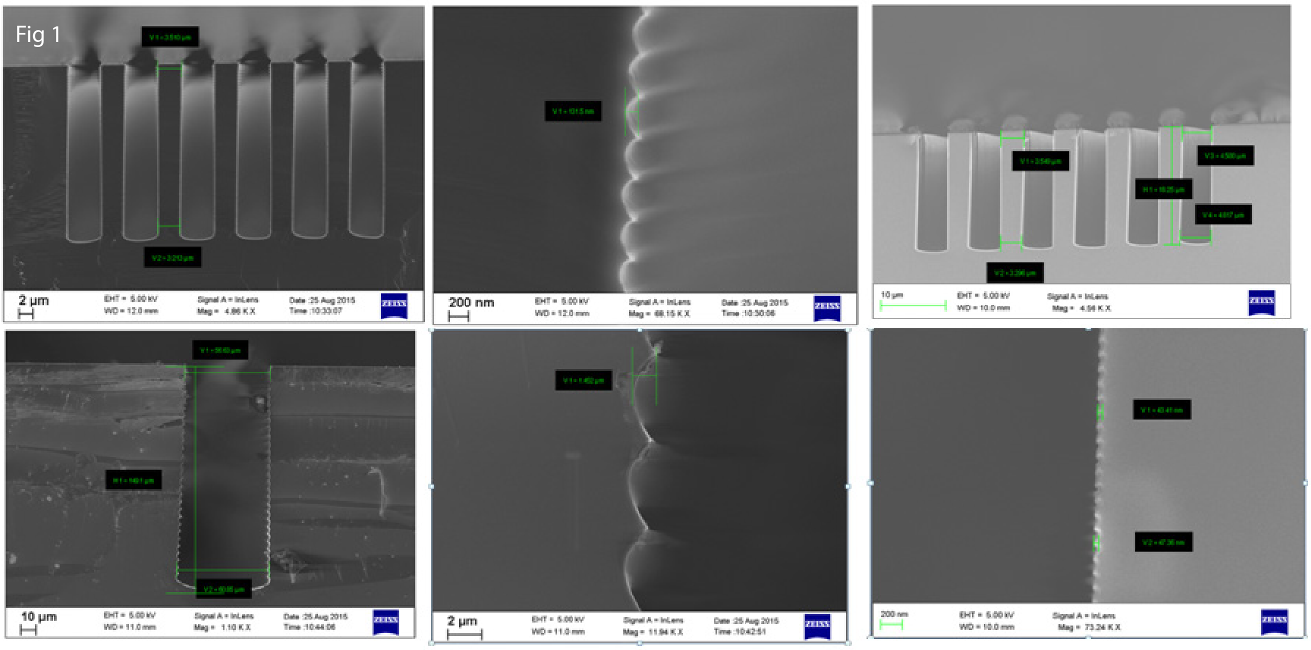


Fig 2

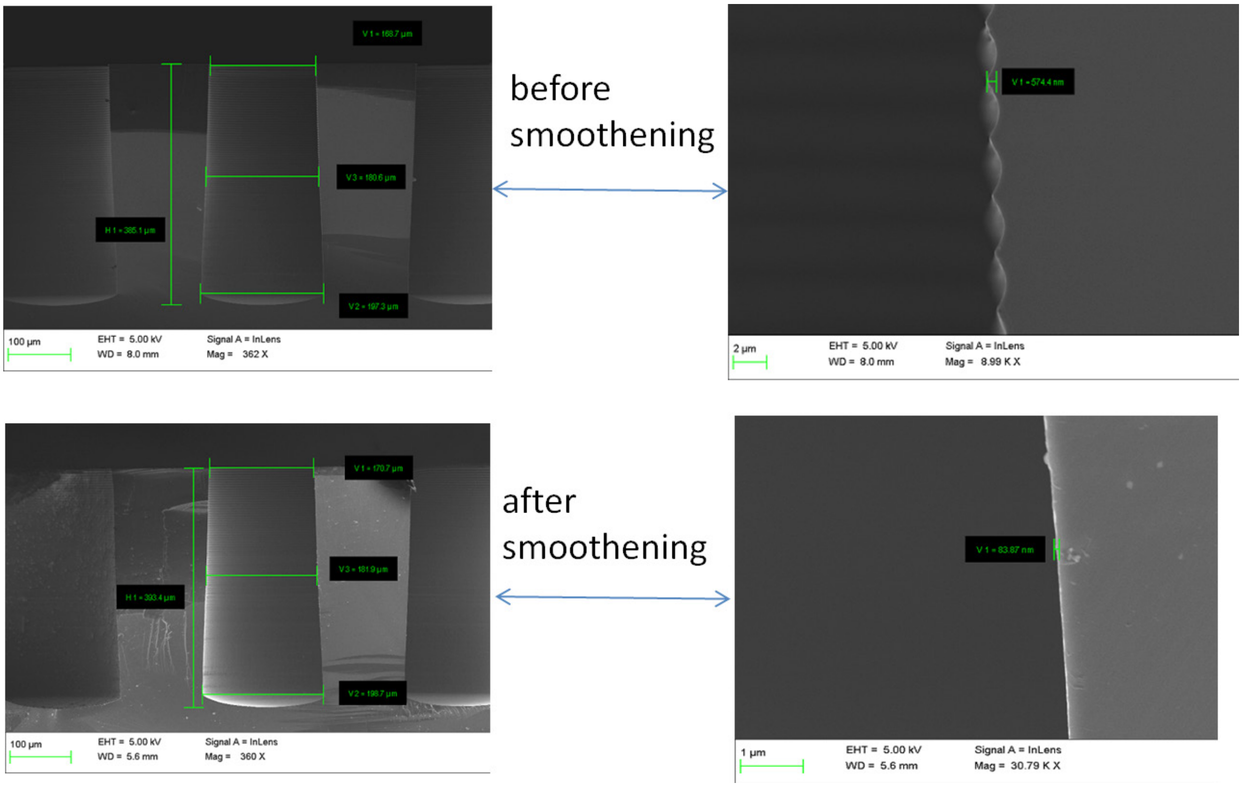
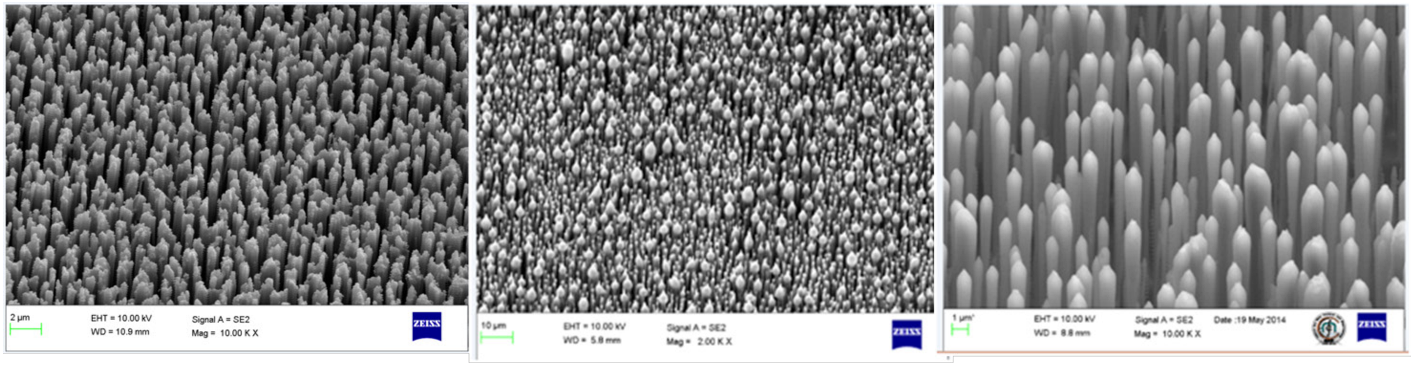


Fig 3

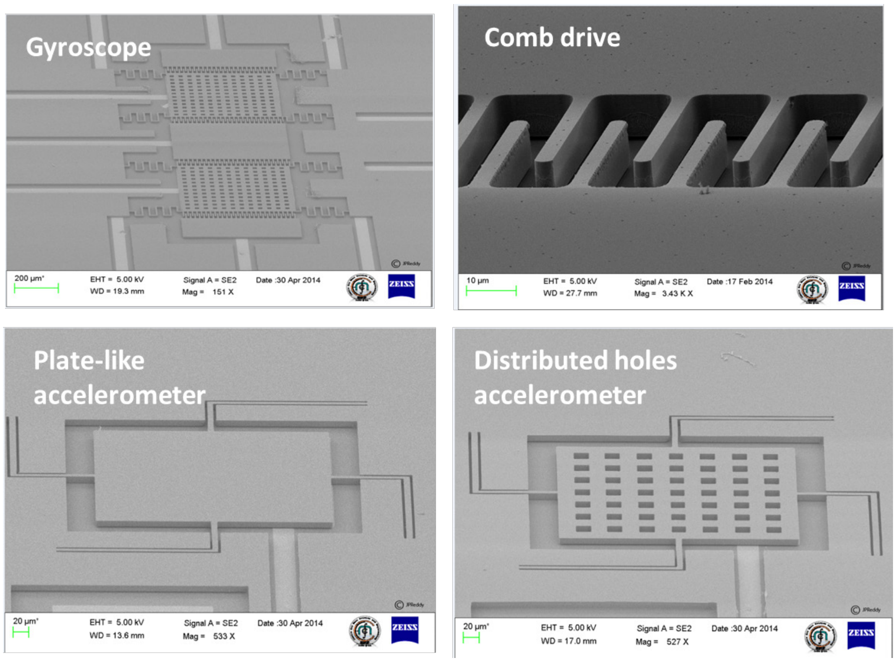


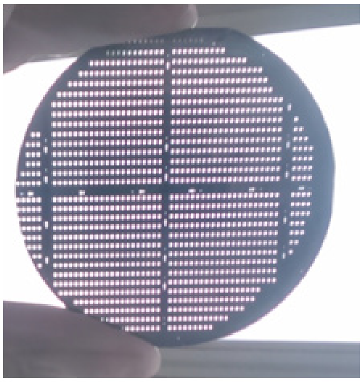
Nanocity effect

DRIE with Zirconia Nanoparticles

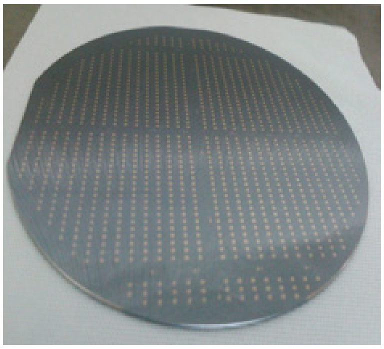
DRIE with Alumina Nanoparticles

Fig 4



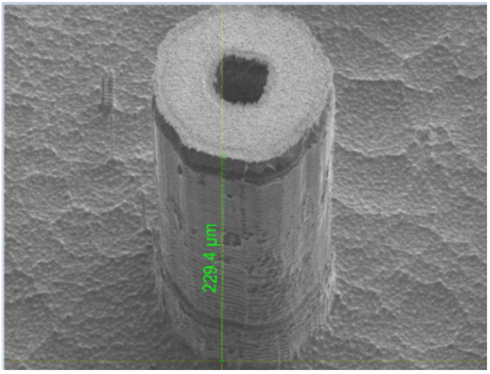


DRIE etched silicon mask



Gold Sputtered on silicon

Fig 5



Facing Page

Fig 1: DRIE process capability, courtesy NNfC team

Fig 2: Scallop smoothening, courtesy NNfC team

Fig 3: Nanostructured surface, courtesy(Micro/Nanofluidics Lab, CeNSE)

Above

Fig 4: Accelerometer/Gyroscope (Courtesy KJP Reddy of Prof. Rudra Pratap's lab)

Fig 5: Microneedles fabricated using DRIE, Courtesy Gopal Hegde, NNfC

create the "nano Hong Kong skyline effect" on silicon, as shown in the adjoining images.

Backside release of membranes and precise landing on oxide membranes has also been achieved for various applications.

Stencil lithography is a novel method of fabricating nanometer-scale patterns using nanostencils which are stencils (shadow mask) with nanometer size apertures. It is a resist-less, simple, parallel nanolithography process, and it does not involve any heat or chemical treatment of the substrates (unlike resist-based techniques). Seen below is a stencil mask generated using our DRIE tool.

Microneedles with lumen and reservoir are being developed for local drug delivery with precise dose in controlled release to overcome the over dosage problem and to reduce side effects.

DRIE is an exciting process, with immense capabilities. We at NNfC would like to work on projects involving the DRIE process. The facilities at NNfC may be used by any researcher from the academia or industry, from within India or abroad. They are fully automated and reservations may be made online. The NNfC maintains an active twiki page: http://www.cense.iisc.ernet.in/nanotwiki.html

Focused Ion Beam at MNCF

B. N. Suma

Fig 1

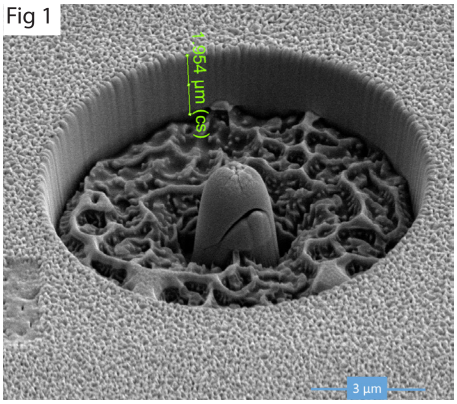


Fig 2

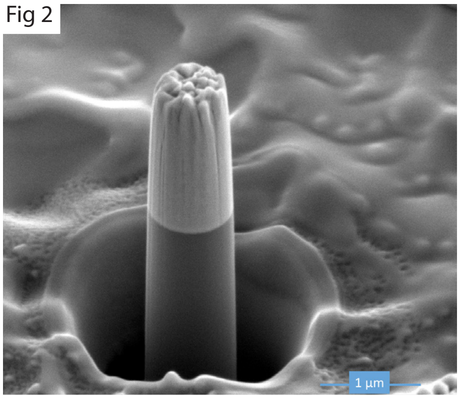
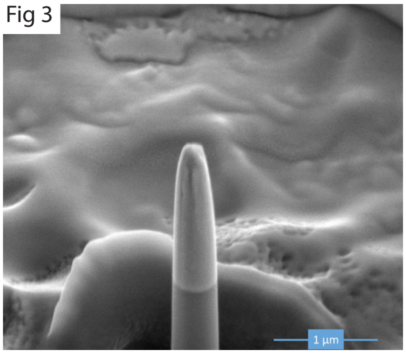


Fig 3



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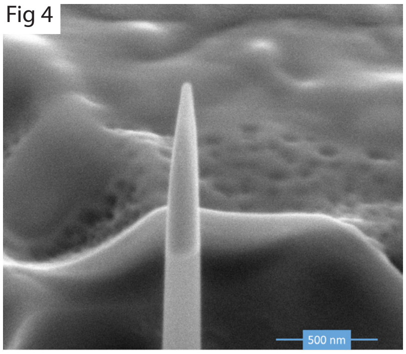


Fig 5

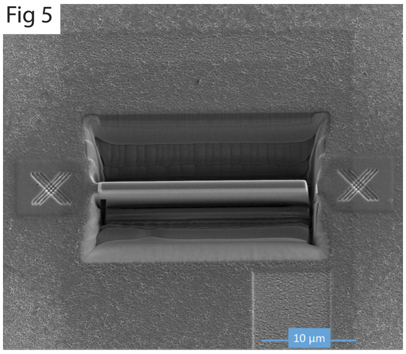


Fig 6

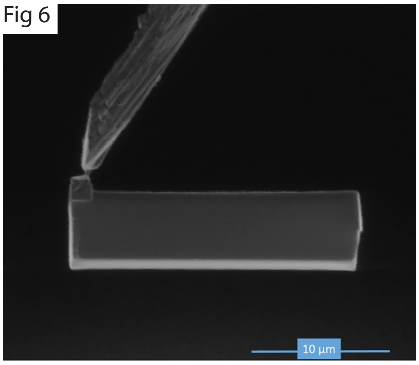


Fig 7

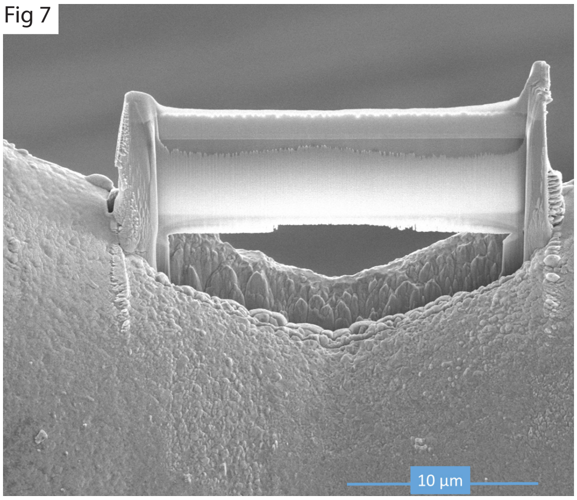


Fig 1: Rough milling of NiMnGa by FIB

Fig 2: Polishing with low ion beam current to avoid cracks on the Pillar (diameter ~1 µm)

Fig 3: Second step of polishing

Fig 4: Final polishing of the pillar retaining the single crystal

Fig 5: Cross-section with Protective film of Platinum

Fig 6: Lift-off using Manipulator

Fig 7: Bird's eye view of a wide, electron-transparent, cross-sectional sample

Fig 8: FEI Helios NanoLab 600i at MNCF

The Micro and Nano Characterization Facility (MNCF) is a centralized facility for characterization of Micro and Nano devices. The MNCF is 5000 sq. ft. precision-controlled environment housing four distinct laboratories for Electrical, Mechanical, Optical and Material Characterization. This national facility with a plethora of high-end equipment spanning multiple disciplines of nano science and engineering rarely found under a single roof. The mission of this facility is to support research and educational objectives of IISc researchers, external academic users, INUP users, Industries and National Laboratories.

The Material Characterization laboratory has tools such as Scanning Electron Microscopes, Focused Ion Beam, and X-ray Photoelectron Spectroscopy for studying different material properties (structural, functional) and material behaviour. The tools are handled by highly trained technical and support staff. The focus of the article is capabilities and achievements using Focused Ion Beam, also known as FIB.

FIB is a technique used particularly in the semiconductor industry for site-specific analysis, deposition, circuit modification, mask repair and transmission electron microscope sample preparation of site-specific locations on integrated circuits, as well as in material science for sub-surface cross-section studies and TEM lamellae preparation. The FEI Helios NanoLab 600i, a Dual Beam system that integrates ions for FIB and an electron beam for SEM functionality.

Capabilities of FIB:

The capabilities of FIB with respect to imaging are: High-resolution electron beam imaging of FIB cross sections can be done without eroding the feature of interest; Sample surface imaging with the electron beam during navigation without erosion or gallium implantation from the ion beam; TEM sample preparation with in situ conductive coating using gas injection system in the system. The potential applications of FIB are: Fabrication of micro- and nano-structures, Circuit edit/device modification, Etching, Process Yield Engineering, and Lithography. Here we present the fabrication of Micro Pillars of NiMnGa (Nickel Manganese Gallium) and TEM lamellae preparation.

Fabrication of Micro Pillars

The main disadvantage of bulk NiMnGa is its brittle nature, which can be overcome by preparing single crystals or deposition in the form of thin films. Preparation of single crystal NiMnGa is very costly and it is very difficult to machine the material for micro-device applications. Thin films on the other hand provides a better solution for brittleness as well as batch fabrication for MEMS devices. Nano-pillars with different aspect ratios (diameter/length) were fabricated using focused ion beam milling to understand the mechanical response of the material at nano and micro-scale.

In detail the NiMnGa pillars fabricated using a dual beam FIB/SEM operated with a Ga+ ion source at 30 keV was applied. The micropillars were fabricated using an ion current of 2.5 nA for coarse milling and a milling current of 230 pA for final polishing.

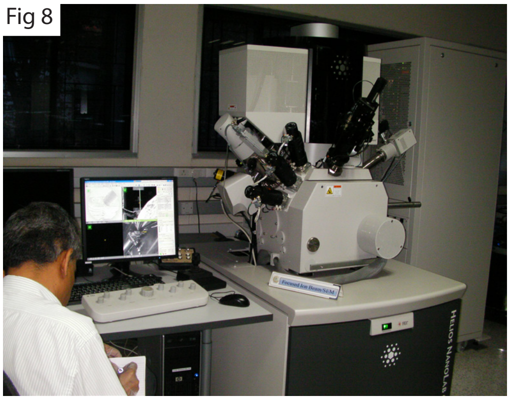
After the final polishing, a single crystal of NiMnGa was obtained.

TEM lamellae preparation:

Gallium nitride on Si substrate is a good candidate material for high power electronics. However, it has a high level of dislocations. The statistical quantification of dislocations in gallium nitride can be done precisely by cross-sectional TEM analysis. But the high hardness of nitrides makes it difficult to prepare cross-sectional TEM samples of GaN by the conventional metallographic method: It is a laborious and time-consuming process. Yet, the resultant electron transparent sample is limited to a width of a few hundred nm. By contrast, FIB is an easier way of preparing cross sectional sample and provides a much wider electron-transparent region, ~20 μm when Ga-ion etching is used. The figure 5, 6, 7 shows the steps involved in the preparation of GaN sample FIB.

Currently, the MNCF website is upgraded for ease of use, up to date tool details, facility information, online manuals, activity tracker, and enhanced payment modes are some key features. Kindly visit www.cense.iisc.ernet.in/mncf.htm for more information.

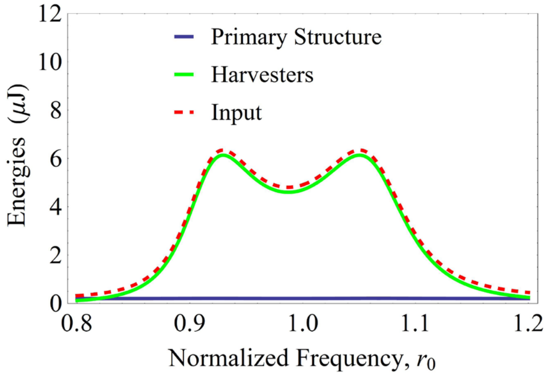
Fig 8



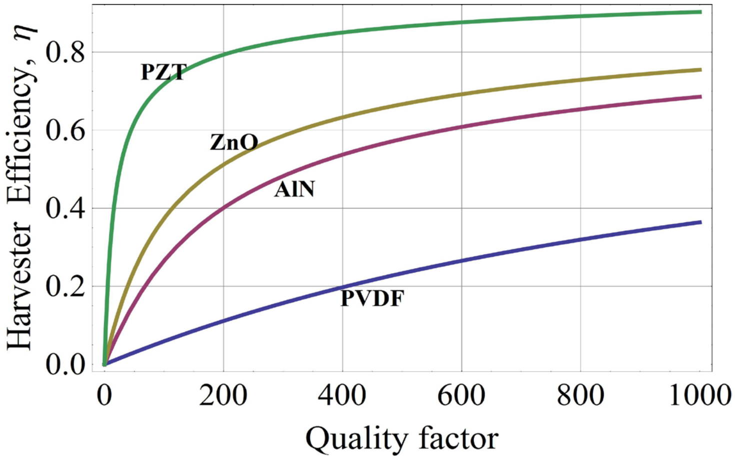
VIBRATIONAL ENERGY HARVESTERS

Harvester Design for Effective Absorption of Vibration Energy

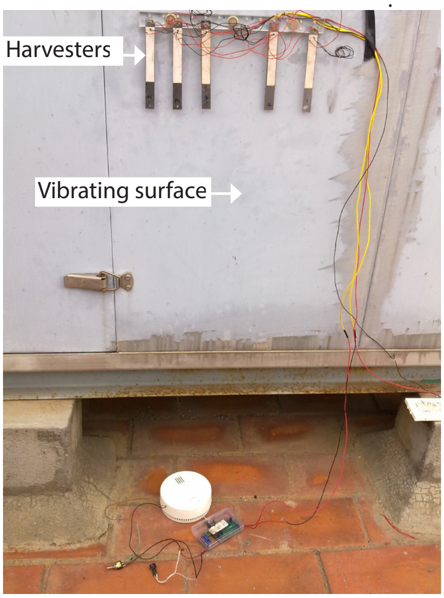
Rammohan Sriramdas



Right: Fig. 1. Optimal characteristics of harvester ensure that much of the energy available at the source is transferred to harvesters.



Above: Fig. 2. Maximum possible efficiencies of harvester as a function of quality factor are shown for four different materials.

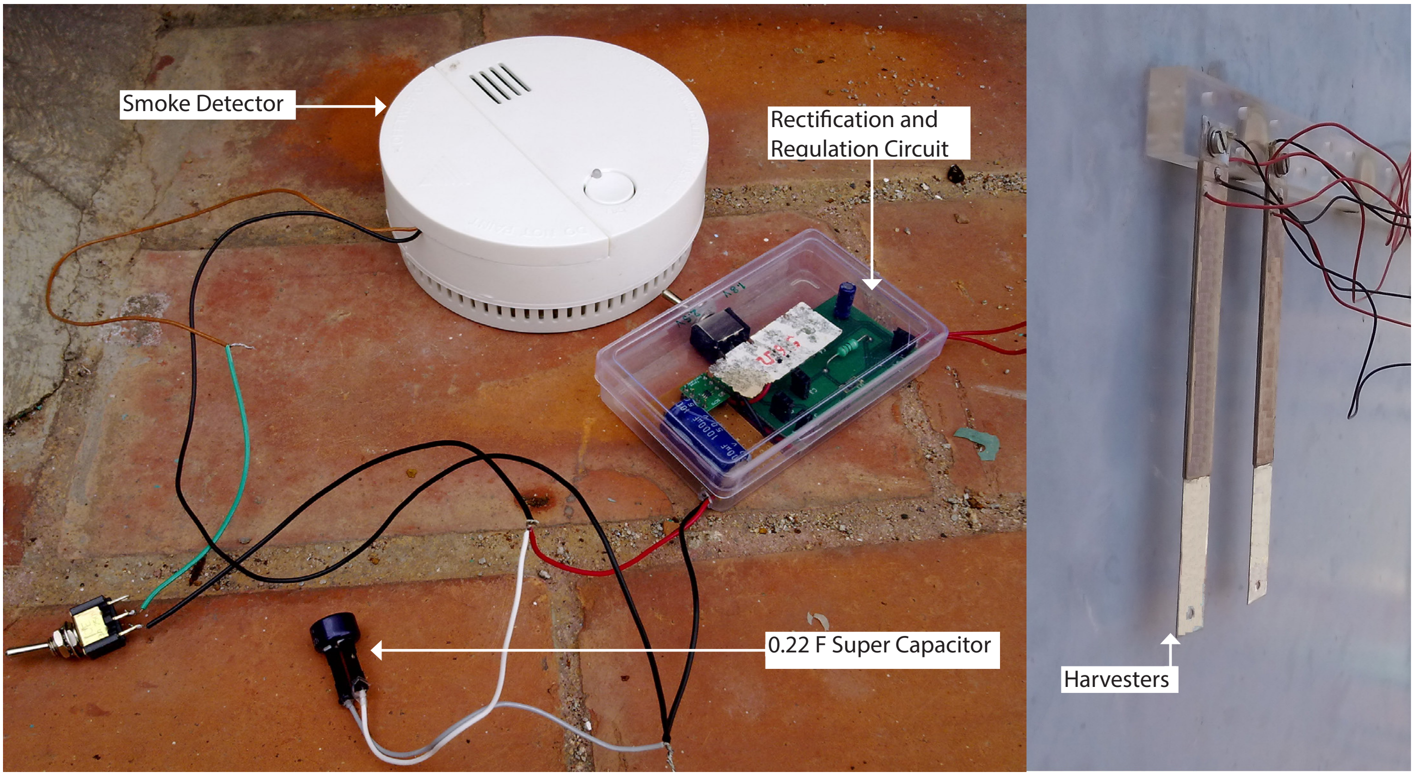


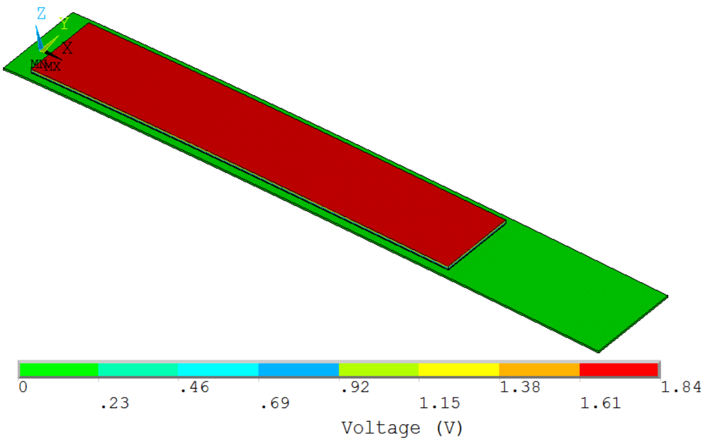
Left: Fig. 4. Smoke detector working on the power that is harvested from vibrations of ducts and blower surfaces in CeNSE.

Energy harvesters are central for powering sensors without batteries. Low-power requirements of contemporary sensing technology attract research on alternate power sources that can replace batteries. Energy harvesters absorbing ambient vibrations function as power sources for sensors and other low-power devices. Improving the performance of these harvesters is pivotal as the energy in ambient vibrations is innately low.

Effectiveness of a harvester in absorbing the ambient vibration energy is determined in two stages. The first stage is the effective transmission of energy from a given vibration source to the harvester and the second stage is the efficient transduction of energy by the harvester to an electrical load. Transmission of energy from a vibration source to a harvester depends significantly on the dynamic characteristics of the harvester. We propose an algorithmic way of determining the harvester characteristics by maximizing the energy transmitted to the harvester [1]. Furthermore, the number of harvesters required for optimal transmission of energy over a considerable bandwidth is also determined. The optimal parameters not only ensure that the energy absorbed by the harvester is maximized but also improve the bandwidth of absorption which is very valuable for energy harvesting. It can be observed from Fig. 1 that, in an optimized system, much of the energy supplied is effectively transferred to the harvesters.

Piezoelectric bimorphs have been shown to be preeminent in converting the mechanical energy in ambient vibrations into electrical energy. We focus on enhancing the performance of piezoelectric harvesters through a multilayer and, in particular, a multistep configuration [2]. We corroborate experimentally that a harvester with





Top: Fig. 4. (Magnified) Smoke detector working on the power that is harvested from vibrations of ducts and blower surfaces in CeNSE.

Above: Fig. 3. The electric potential distribution computed using ANSYS software for a PZT harvester having optimal mechanical architecture is shown.

References:

[1] Rammohan S, Shreevar R, Rudra Pratap. Design Considerations for Optimal Absorption of Energy from a Vibration Source by an Array of Harvesters. 10th Energy Harvesting Workshop, Virginia Tech, Blacksburg. (2015).

[2] Rammohan S, Sanketh Chiplunkar, Ramya M Cuduvally, and Rudra Pratap. Performance Enhancement of Piezoelectric Energy Harvesters using Multilayer and Multistep Beam Configurations. IEEE Sensors Journal 15(6): 3338–3348 (2015).

multistep configuration yields almost 90% more power than that from a multilayer configuration when both are made out of the same volume of piezoelectric material. The modeling methodology described in [2] is extended to determine the maximum possible efficiency of transduction for a bimorph harvester. The efficiency of a harvester depends on the coupling factor that in turn depends on the geometry and the material. The coupling factor is maximized with respect to geometry of theharvester by selecting appropriate thickness and Youngs modulus for both passive and active layers of the harvester. Additionally, the efficiency is observed to depend significantly on the harvester's quality factor. Depending on the chosen piezoelectric material, there exists an upper limit for harvester efficiency. The distribution of maximum possible efficiencies for four different piezoelectric materials as a function of quality factor is shown in Fig. 2. Finite element simulations are also performed on a geometrically optimized PZT harvester. The electric potential distribution on the harvester across 100 kΩ resistance for 0.1 g input at 34 Hz is shown in Fig. 3. The power generated by the harvester is observed to be sufficient to turn ON an off-the-shelf smoke detector (Fig. 4). The smoke detector in the present case requires 60 μW for normal operation and 8 mW for smoke alarm ON. Although PZT has been in common use for energy harvesting, research on lead-free piezoelectric materials, viz., Barium Titanate and Potassium Sodium Niobate, is gaining impetus. We are currently studying AlN- and ZnO-based harvesters for their potential as micro harvesters.

Graphene - Paper Gas Sensors

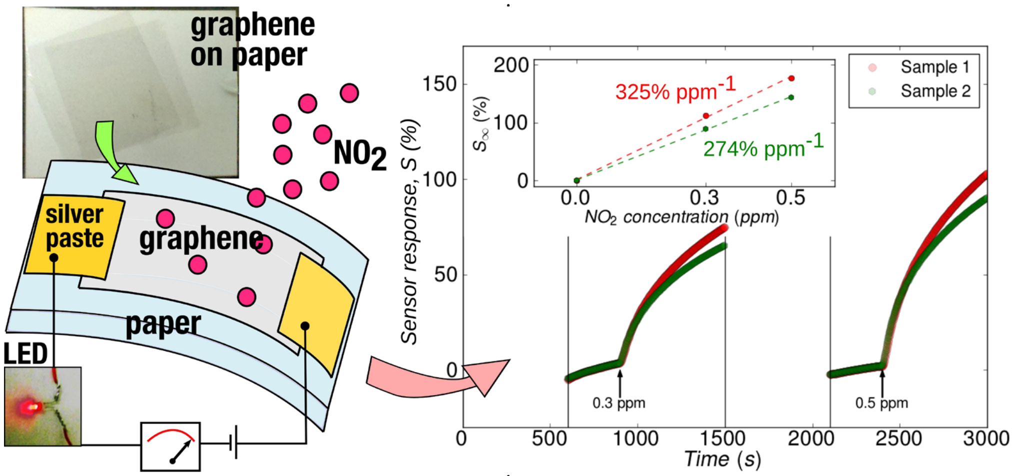
Shishir Kumar, Swati Kaushik, Rudra Pratap and Srinivasan Raghavan

A large part of the developing world, including India, can enjoy a better quality of life if chemical sensors become low-cost and accessible. Glucose-testing strips are a great example of how an easy-to-use, low-cost method can transform the lives of millions. Agricultural and environmental monitoring are two other areas where such devices will make a wide impact. Our work on graphene-based gas sensors on paper is a step in this direction [1]. As the readers may know, graphene is a single atomic layer of graphite. Because all of the atoms of graphene are exposed to external influences, and because some of its physical properties, graphene can be used to make very sensitive chemical sensors. And depending on how we modify it, it can be used to sense many different chemicals. Paper, on the other hand, is abundant, eco-friendly and easy to process. Thus, if we can assemble the graphene sensor on paper, it will be a win-win for consumer-level sensing.

Graphene-paper devices (see Figure) do exactly that. We have laid out a strip of graphene on paper, taking care that it is not damaged in the transfer. Silver paint was applied to the ends of the strips to make electrical contact. This gives us a resistive gas-sensor, i.e., one whose resistance changes appreciably when certain gases come in contact with it.

Thus, to measure the response of the sensors, one only needs to monitor resistance of the strip, which leads to a very simple and robust system. The energy spent on a measurement is also quite low, as the resistance of a graphene strip is quite small.

G-paper sensors can sense NO2 (a health hazard) to as low as 1 ppb (parts per billion), which is better than most commercially available sensors (see Figure). Two other metrics of concern are how fast the sensor responds to the test gas, and how fast it recovers when the test gas is removed. For the former, G-paper sensors are almost as fast as commercial sensors, and for the latter we found that a deep ultra-violet treatment makes the recovery almost instantaneous.



A photograph of two layers of graphene transferred on a paper sheet. (Left bottom) Schematic of a G-paper device, showing that the device can sustain enough current for an LED. When exposed to NO2 gas, the percentage change in resistance of the strip can measured. This is shown in the plot on the right. The arrows denote when the test gas was introduced to the sensor. The inset to the plot shows the overall change in sensor response as it is exposed to different concentrations of NO2 gas.

We went on to show that these sensors are also flexible and the strain can be used as another lever to tune sensing performance.

In future, we would like to modify graphene to sense many more gases and chemicals. Using arrays of modified graphene sensors, we expect to identify the composition of the air on a busy road. We also would like to make a complete sensing system on paper itself so that the cost reduces even further.

References:

1. Kumar, S et al., Graphene on Paper: A Simple, Low-Cost Chemical Sensing Platform. ACS Appl. Mater. Interfaces 7, 2189–2194 (2015).

Φρεσηερσ (freshers) 2015

It was a proud moment for us when 38 young and brilliant minds joined the CeNSE family. The freshmen were invited for an enthralling interaction session followed by celebratory

dinner. With the philosophy "Let's make some sense out of CeNSE", Prof. Rudra Pratap inaugurated the event and urged the CeNSE family to assume leadership.

The motivating speech was followed by a welcome gift to the freshmen. The gift was sponsored by IEEE Joint Student Chapter NC NS. IEEE Student Chair Neelima talked about the benefits of joining the IEEE Student Chapter and encouraged the freshmen to be a part of it. The IEEE CeNSE Student Chapter plans to organize events throughout the year.

The event captured attention with a remarkable Teacher's Day celebration. The organizers came up with a quiz – Have you met our professors!! The professors were introduced with something unique to each of them and were gifted a caricature resembling them.

Goodbyes are never easy, are they? On the one hand, we have freshmen joining us and on the other, we have students graduating from our family. We had nine PhD students who have submitted their theses. The graduating students were honoured by books gifted to them by their advisors. The advisors and the students shared some funny and inspiring experiences together.

Prof Navakanta Bhat shared the most inspiring story of his student Vinay Kumar Chauhan, who completed his PhD in just 2 years. Vinay, suffering from Diabetes from the age of 14, took upon himself to fight his own battle. He has started his own company which deals with Diabetes healthcare.

The first half of the event was celebrated by a delicious chocolate cake and high tea.

The second half of the event involved interaction with the freshmen over a series of games and activities. We discovered that our new family members are not just brilliant minds but are superb entertainers as well. We hope that they take their hobbies and passions to great heights and keep dazzling us and the world in the future. The event was concluded with a celebratory dinner. It was indeed a CeNSEational event.

EVENTS AND ANNOUNCEMENTS

Seminars

July

"Scalable Nanomanufacturing of Carbon/ Nanocarbon- based Supercapacitors for Next Generation Energy Storage" by Prof. Apparao M. Rao, 8th July

"Nanoscale Hybrids: A Microscopic Investigation of the Surface/Interface and their Emerging Potential in Neuroscience" by Dr. Paromita Kundu, 14th July

"Electrochemical field-effect & ion-exchange: Towards innovative control of material properties" by Dr. Subho Dasgupta, 16th July

"Emergent Active Colloids and Computational Fluids" by Dr. Madan Rao, 23rd July

"Controlling defects in CVD-grown graphene; A device performance perspective" thesis colloquium by Krishna Bharadwaj B, 24th July

"Point-of-care Electrochemical Detection of Biomarkers for Diabetes and its Complications" thesis colloquium by Vinay Kumar Chauhan, 27th July

Aug

"Plasmon-enhanced Thin Film Amorphous Silicon Photovoltaics" by Dr. Keyur Gandhi, 3rd August

"Dissipationless spin currents: From fundamentals to functional devices" by Dr. Niladri Banerjee,13th August

"A Cellular Solution to an Information Processing Problem" by Prof. Garud N. Iyengar, 20th August

Lecture as a part of the CeNSE Course NE-101, Entrepreneurship, Ethics, and Social Impact by Sri M.N. Vidyashankar, Former Additional Chief Secretary, Govt. of Karnataka, 26th August

"Probing the Physical World with Extremely Small Scale Oscillations" by Prof. Rudra Pratap, 27th August

Sept

"Nanoscience and Materials Engineering Approaches to Electrochemical Energy Storage and Solar Energy Conversion" by Dr. Vinodkumar Etacheri, 3rd September

"Freestanding Silicon Nanomembranes for Pure and Applied Physics" by Dr. Gokul Gopalakrishnan, 18th September

"Electron transfer dynamics in photoelectrochemical solar cells" by Dr. Aravind Kumar Chandiran, 22nd September

Lecture as a part of the CeNSE Course NE-101, Entrepreneurship, Ethics, and Social Impact by Mr. Parag Dhol MD, Inventus Capital Partners, Bangalore & Silicon Valley, USA, 23th September

"Assisted Self-Assembly for Large Area Nanopatterning" by Dr. Sridhar Krishnaswamy, 24th September

"Computational imaging of nanoscale order in living systems with fluorescence polarization" by Dr. Shalin Mehta, 28th September

Workshops

INUP Hands-on Training Workshop, 2-10th July

Digital India Workshop, 4th July

INUP Familiarization Workshop, 20-22nd July

INUP Hands-on Training Workshop, 3-11th August

NPMASS Exhibition, 22nd August

CeNSE Fresher's Day, 11th September

Announcements

SanDisk joins CeNSE Industry Affiliate Program, the inaugural meeting was held at CeNSE on 7th July.

BCausE Enterprise joins Indian Startup Affiliate Program: the inaugural meeting was held at CeNSE on 17th July.

Anish Roychowdhury wins the Best Paper Award at the 6th International Conference on Computational Methods, Auckland, New Zealand, July 14-17 for the paper titled "Development of microsystems analysis software using hybrid finite elements and direct solution of coupled equations"

Rammohan's paper in IEEE Sensors Journal titled "Performance enhancement of piezoelectric energy harvesters using multilayer and multistep beam configurations" makes it to the top 50 downloaded papers among 4000 papers published by the Journal (Vol. 15, No. 6, June 2015).

Special visitors to CeNSE on 11th September:

Mr François Gautier, The Consulate General of France in Bangalore,

French Optics and photonics competitiveness cluster delegation,

Science Department of French Embassy in India, Business France,

Karnataka State Council for Science & Technology

For Upcoming events:

Visit www.cense.iisc.ernet.in/news_events.htm

CeNSE welcomes the 2015 batch

Photo by R. Dwarakanathan

CeNSE newsletter is published quarterly by the Centre for Nano Science and Engineering to keep the community of academia, industry, and government organizations informed of its activities and accomplishments.

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