CeNSE newsletter

October – December 2014 | Volume 1 | Issue 1

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Message from the Chairperson

Rudra Pratap

A decade ago, a few of us from different disciplines and departments of the Institute embarked on what appeared to be a very ambitious project: to build a state-of-the-art laboratory in which structures and devices on the micro and nano scale could be designed, fabricated, and investigated, where new technologies and products could be developed to meet the relevant needs of the country. It was not just the size of funding required that was the deterrent, but daunting indeed was a lack of local expertise and experience, the size and complexity of the venture, the need for sustained and intense effort for several years (without tangible academic output). What was then a gleam in our eyes is today a slew of gleaming laboratories, anchored by the National Nanofabrication Centre (NNfC) and the Micro Nano Characterization Facility (MNCF), both fit enough to set standards for academic institutions anywhere.

Thanks to the tremendous support and funding we have received from the Institute and from agencies of the Government, we have today a new academic entity, the **Centre for Nano Science and Engineering**, housing excellent R&D infrastructure, beckoning and available to researchers from within the Institute and beyond. While this is only the beginning, the events and experience since 2012 (when the NNfC and MNCF became fully operational) instil confidence in us that, together, we are well on the way to realizing the ambitious vision that got us started. We have well over one hundred students of the Institute working every day in the CeNSE labs for their PhD theses, fabricating devices on a fine scale and investigating phenomena on the nanoscale.

The Industry Affiliate Program, through which we intend to have close engagement and collaboration with the high-tech industry, has attracted seven stalwart companies – companies with global presence – who have begun to work with us for mutual advantage. Agencies of the Government with responsibility to meet the strategic needs of the country are joining hands with us to find creative solutions to demanding problems. Among these is the design, fabrication, testing, packaging, *and delivery* of a range of pressure sensors with exacting specifications, all carried out during the last one year at CeNSE through the fusion of in-house capabilities and expertise.

Capping it all has been the gratifying experience of the Indian Nanoelectronics Users Program (INUP), through which the facilities of the Centre have been made available for the hands-on training of academic researchers from around the country. Following the training, these researchers carry out their research projects at CeNSE, all expenses paid, with help and guidance from the experts at CeNSE. INUP has been received extremely well by the research community, and has thus greatly exceeded the goals set for the Program, attracting participation by more than fifteen hundred researchers from about 150 institutions spread far and wide. The Program has underscored the effectiveness of national facilities in training researchers, advancing R&D in smaller institutions, fostering collaboration and, indeed, improving classroom instruction because teachers have now gained first-hand experience with devices and device-making.

The Centre has launched a two-year M.Tech. programme, providing intensive training in the classroom and the laboratory to a select few. A program of summer internship has been much sought-after by the brightest young students of the country.

All this amounts to a very active and busy CeNSE, with much happening and being accomplished. Hence this newsletter, through which we intend to keep you abreast of the R&D being conducted at CeNSE, the technologies developed (and deployed), the results of research as our students and their mentors explore the nano domain. We thank you for your support even as we invite you to join hands with us in the journey.

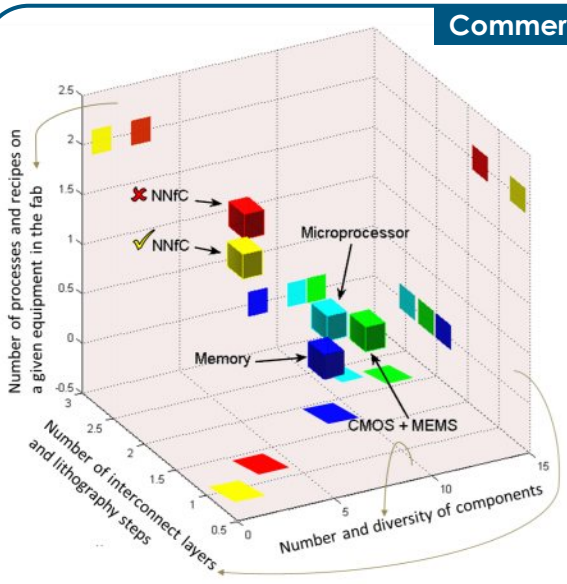
Faculty Insights: National Nanofabrication Centre (NNfC) at CeNSE: The Right Perspective

Navakanta Bhat

For a long while, I was thinking about the appropriate topic to write this article for the inaugural issue. Should it be a reflection on our 12 year long, exciting journey which culminated into the unique feature of CeNSE today– National Nanofabrication Centre (NNfC), one of the finest Nanofabrication facilities in the world, in an university setting. How about the new device technologies that have been created in NNfC, in a very short span? Or should it be our vision for the Nanofab over the next decade? Then I thought, it is perhaps appropriate to articulate the differences between NNfC and a commercial Silicon fab producing "chips", with a labelled "technology node".

While every visitor to NNfC has been awestruck with the facility, most of them, including our own students, have often asked me a few related questions – What "technology node" do you have (…90nm/65nm/ 45nm /32nm/22nm…) ?
Is it possible to get the chip designs fabricated in your "foundry"? What kind of yield do you get in the fab? Most of these questions are due to the view point arising from news items on silicon CMOS foundries announcing electronics chips on new technology nodes once every 2 to 3 years. This perspective is conditioned by players like Intel, TSMC, Samsung, Global Foundries.
The process yield of a fab refers to the percentage of working devices, out of the total number of devices fabricated. The yield of the fab is inversely related to the defect density (number of defects per unit area of wafer) introduced during the processing of the wafer/substrate in the fab.
It is instructive to look at the 4-dimensional graph that depicts the yield and hence the characteristic features of a fab. The three axes represent (i) Number and diversity of components, (ii) Number of interconnect layers and lithography steps (iii) Number of processes and recipes on a given equipment in the fab. In general, the defect density increases exponentially with increase in any of these 3 variables. The 4th dimension illustrated through colour code is the percentage yield. In general, defect density increases exponentially with increase in any of these 3 variables.

Commercial fabs versus NNfC



	Number and diversity of components	Number of interconnect layers and lithography steps	Number of processes and recipes on a given equipment in the fab	Yield
Memory	9	1.9	0	~100%
Microprocessor	11	2.5	0	~60%
CMOS + MEMS	12	2.2	0	~50%
✓ NNfC	1	0.7	2	~30%
✗ NNfC	3	1.3	2	~0%

- All the numbers in the first 3 columns are exponents of 10. Ex: A value of 0 in 3rd column indicates 10^0=1 recipe per equipment.
- The values in first column are derived from a composite metric based on number and diversity of components on a chip
- The values in second column are derived from a composite metric based on number of interconnects and lithography steps

Research fabs in general tend to be extremely flexible in terms of diversity of substrates, components and number of process recipes on any given equipment. Change is in the air in fabs like NNfC, and nothing stays constant! While this is an extremely important prerequisite for new innovations in materials, processes, and devices, the flipside is an exorbitantly high defect density in such fabs. Hence any attempt to make a chip with even modest number of components results in near zero yield, since the chip would fail even if one component malfunctions due to high defect density. Hence, research fabs focus on creating new technologies for materials, processes, and devices, but do not build circuits – even ones with a modest complexity.

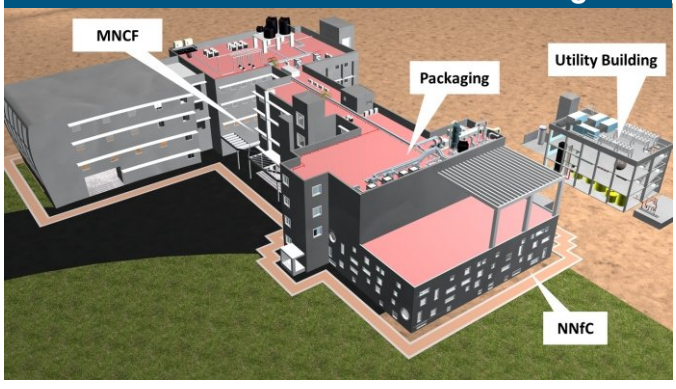
This point can be further elucidated by looking at the difference in yield for commercial fabs manufacturing different chips. For example, memory chip fabs (say DRAM), can achieve close to 100% yield, but the yield in microprocessor fabs is substantially lower. This is because memory chips have identical building blocks (transistors of same dimension) arranged in a systematic array, with very low "diversity of components". In addition, because of the regularity in the layout, memory chips require very few "interconnect layers" (as low as 3 to 4). On the contrary, microprocessors have diverse building blocks (and hence transistors of varied dimensions) indicating "high diversity".

Furthermore, the microprocessors are "interconnect intensive" (as many as 10 or more layers). If a commercial fab attempts to integrate even more diverse components such as MEMS and CMOS on the same chip, the yield will again suffer. Hence, most of the MEMS sensors adopt a System-in-Package solution as opposed to a System-on-Chip (single die) solution. Thus, the right perspective for NNfC is the creation new technologies with a small number of components and low diversity on the chip, to achieve a low to moderate yield.

Since no circuits are made in fabs like NNfC, the definition of the technology node is a moot point. The technology node in CMOS fabs is in the context of building VLSI circuits which, in turn, is related to the (half) pitch and dimension of transistors in the circuit. However, it should be noted that NNfC can outperform commercial fabs in terms of achieving the lowest dimension for any component, due to the utilization of Electron Beam Lithography (EBL) as opposed to Optical Lithography in commercial fabs. For instance, the current state-of-the-art CMOS technology can build transistors down to the gate length of 22nm using 196nm Deep-UV (DUV) source, while NNfC can build transistors down to a gate length of 5 nm using a 30 keV energy electron beam.

In summary, NNfC offers an extremely flexible fab, which enables researchers to innovate new technologies in areas as diverse as CMOS, MEMS, Photonics, Power Electronics, Neuroelectronics, to name a few. In addition, NNfC also supports a wide range of substrates – Silicon, GaN and other compound semiconductors, Glass, Polymers - to be processed under a single roof, which is unimaginable in a commercial foundry. The novel technologies developed at NNfC can subsequently be transferred to appropriate commercial fabs for large scale production of circuits and components with high yield.

CeNSE facilities illustrated in a 3D image



NNfC Updates: Process Integration Capabilities at CeNSE

Sadanand Deshpande

The National Nanofabrication Centre (NNfC) at the Centre for Nano Science and Engineering (CeNSE) is a CMOS/MEMS/NEMS- capable research facility located at the Indian Institute of Science, Bengaluru (India). This Centre houses state-of-the-art research equipment for both fabrication and in-line characterization of the devices.

The Nanofab is capable of routinely processing100mm (4-inch) silicon wafers with a handful of tools that can process larger, 150mm (6-inch) substrates.

A view of NNfC

The NNfC has a dedicated staff of nearly 50 engineers and technicians who maintain the process tools and develop unit process modules to support complex process integration for research and prototyping. At CeNSE, we also have access to test and packaging laboratories that can be utilized to characterize and calibrate devices such as MEMS - based RF switches, pressure sensors, gyroscopes, gas sensors and micro-fluidic devices, to name a few. The NNfC has now been fully operational for almost three years, having opened its doors in January 2012. The details of NNfC construction are available as a valuable resource through the CeNSE YouTube channel (http://www.youtube.com/censeiisc).

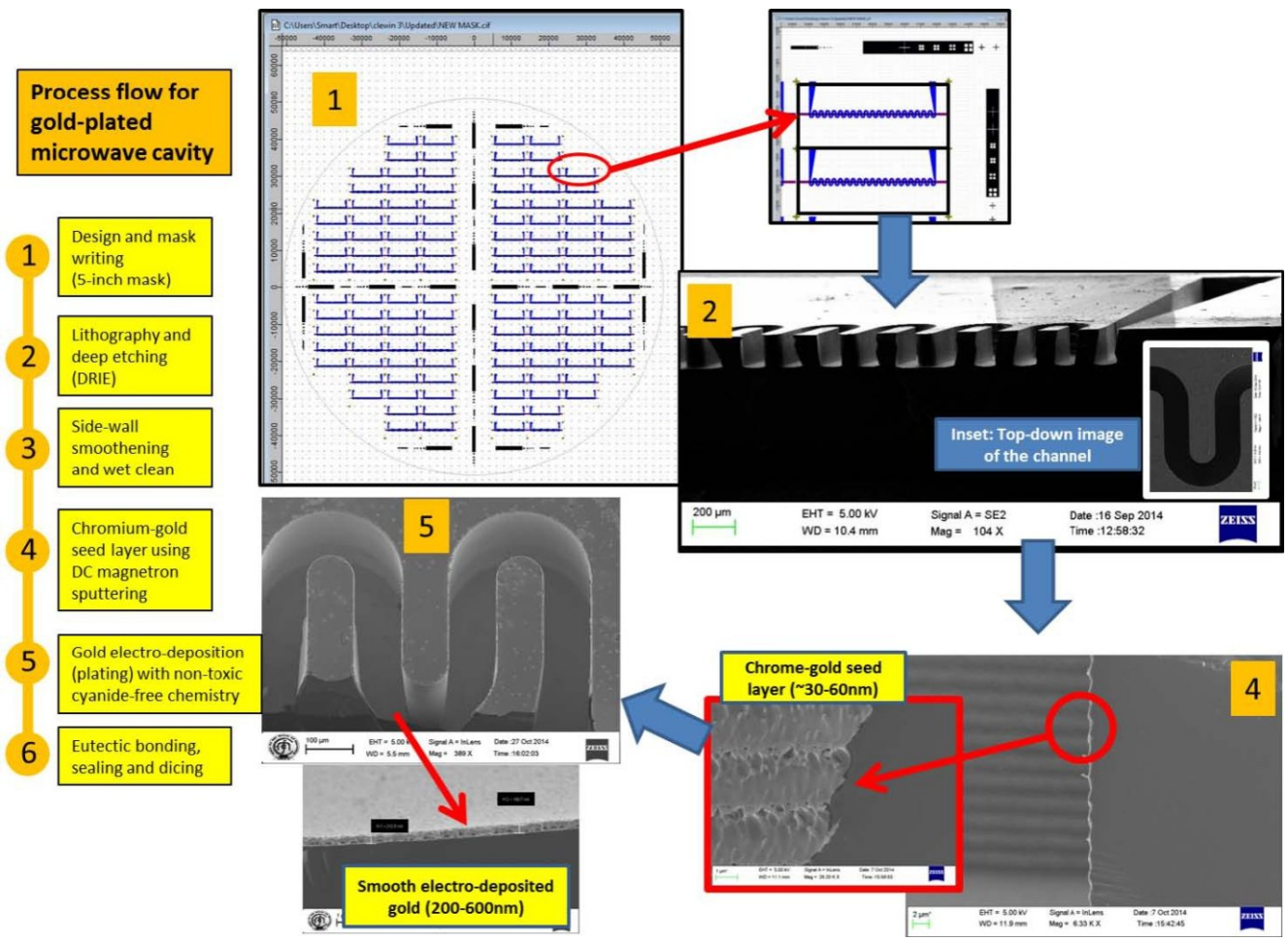
We have developed several unit processes that involve most of the standard semiconductor operations, starting with optical and eBeam lithography, thin film deposition (ALD, CVD, LPCVD, PECVD), dry etching (RIE, DRIE), thermal processing (oxidation, diffusion), electro-deposition and finally, bonding/dicing & packaging.

We are now taking our research efforts at NNfC to the next level by engaging in process integration of more complex process steps that will involve several lithography mask levels and final device or module prototyping. The panel below illustrates our process integration capability for the fabrication of a microwave cavity device. At our Centre, we have also fabricated novel silicon-carbide cantilever structures, electromechanical acoustic and RF MEMS devices, micro- and nano-machined structures, a full range of pressure sensors (0-400 bar), and even biomedical devices such as micro-needles for insulin delivery. Also seen below is an example of electro-mechanical characterization of a RF MEMS switch using the Laser Doppler Vibrometry technique available at CeNSE. The NNfC staff and scientists also have expertise in building equipment to address non-standard unit modules that are needed in a research facility such as ours. Shown below is one such instrument built by our Centre for scaling up electro-deposition of gold and copper for four-inch wafers. In addition, there are multiple research efforts in silicon-photonics, Neuroelectronics, Photovoltaics, Microfluidics and Compound semiconductor-based devices for both commercial and strategic applications.

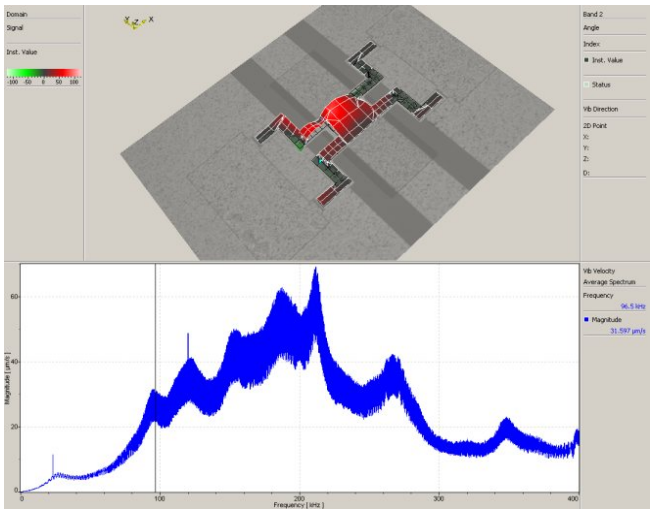
Facilities at NNfC may be used by any researcher from academic or industry, from written India or aboard. They are fully automated and reservations may be made on-line. The NNfC maintains an active twiki page with useful information.

http://www.cense.iisc.ernet.in/nanotwiki.html

Fully integrated process flow for gold-plated microwave cavity device



Novel RF MEMS switch for high frequency applications. Shown below is a Laser Doppler Vibrometer (LDV) frequency measurement of a thin film electromechanical switch.



Electroplating instrument developed at NNfC by for electrodeposition of gold and copper on substrates up to 4 inches in size. This set-up was developed as part of the unit module capability enhancement in the NNfC.

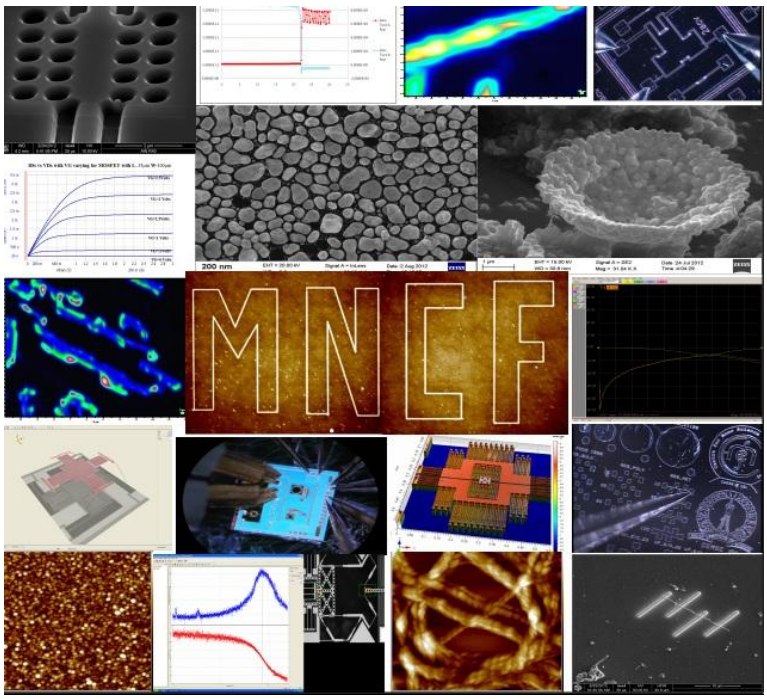
The process integration team at NNfC has been working with partners from the academia, the strategic sector, and industry. We already have several funded projects under way with these external agencies. We are eager to take on more challenging projects with long-term collaboration in mind to enable design validation and prototyping of micro and nano devices "**developed in India**".

MNCF Updates: Characterization capabilities at CeNSE

Girish Kunte and Chandra Shekhar Prajapati

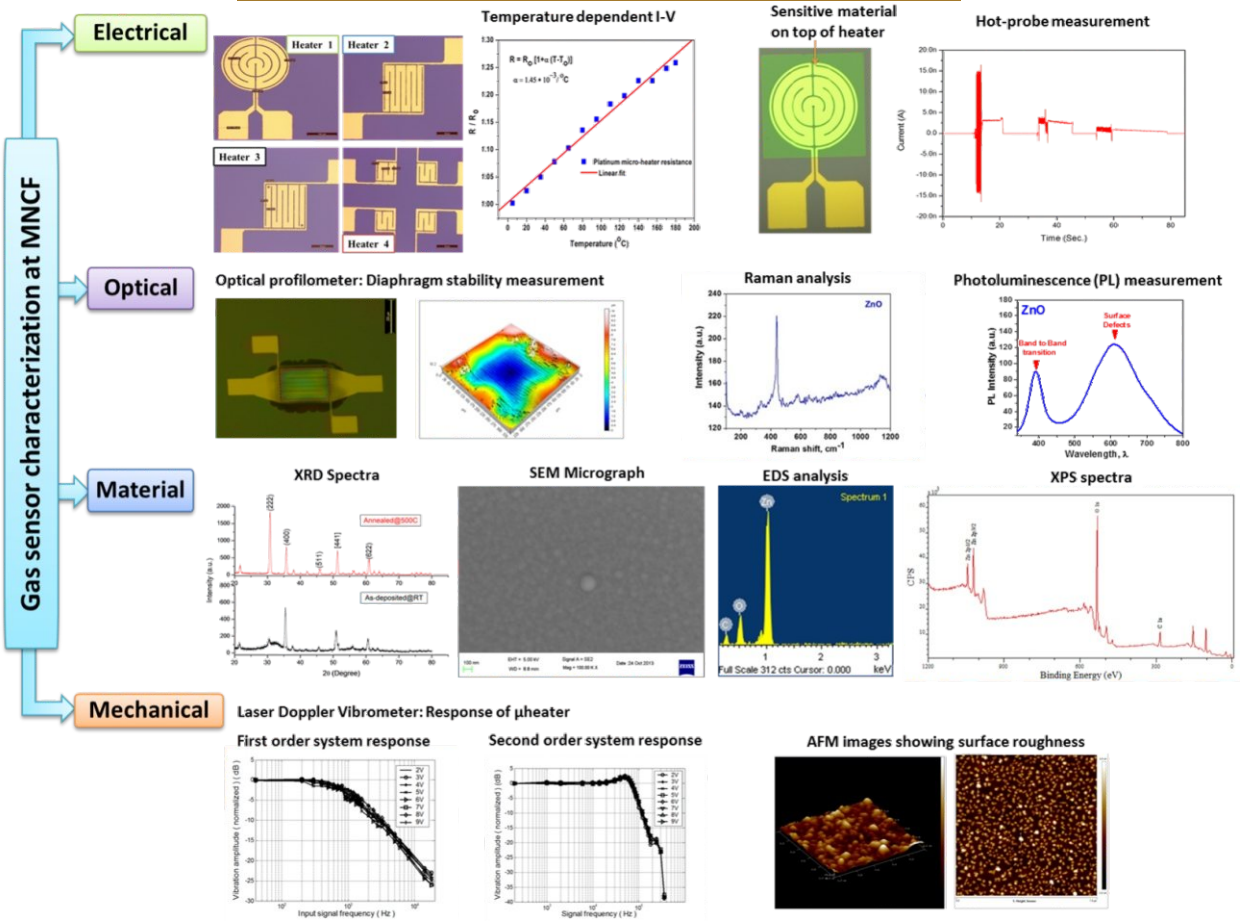
The Micro and Nano Characterization Facility (MNCF) is a 5,000 sq. ft. precision-controlled characterization facility at the Centre for Nano Science and Engineering, IISc. This is perhaps one of its kind in the world, with the greatest diversity of equipment under one roof. The facility comprises four suites of equipment for electrical, mechanical, optical and materials characterization.

In general, characterization is a process of identifying and qualifying the properties or behaviour of a material or a device. At MNCF, a comprehensive characterization is carried out on a wide variety of materials and electronic/ MEMS devices under one roof.



Devices characterized at MNCF include pressure sensors, gas sensors, MEMS devices, RF switches and many more. The complete characterization of gas sensors at MNCF, which portrays the capabilities of the state-of-the-art facility, is illustrated below.

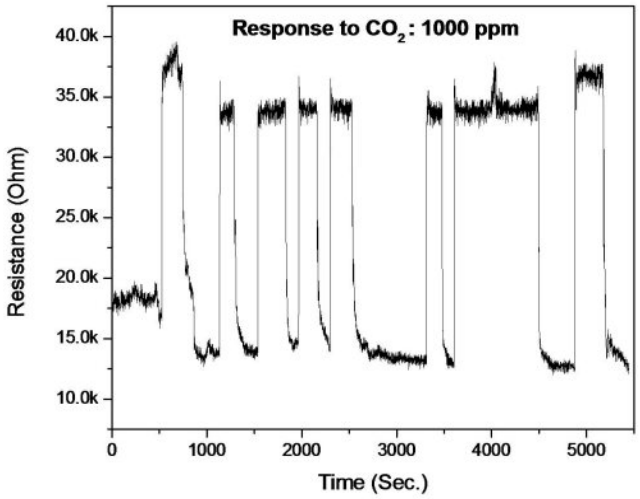
Complete characterization of gas sensors at MNCF

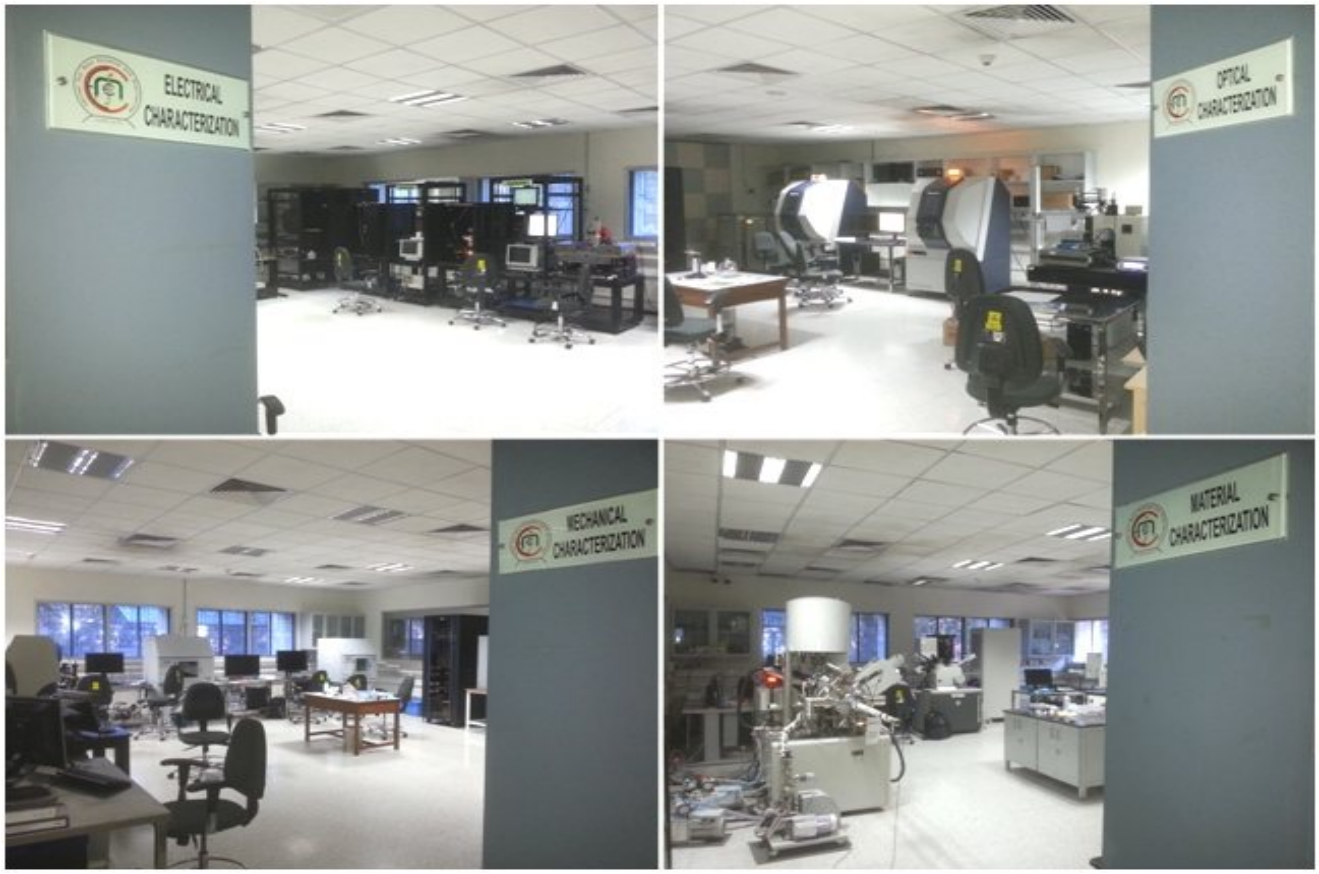


After a detailed analysis of the sensing element in the MNCF, a gas sensor, for example, is packaged and tested comprehensively for its ability to sense the target gas before being deployed in the field.

Packaged CO_2 Gas sensor

Response graph of Co_2





MNCF was established in 2011 to cater to the characterization needs of researchers at CeNSE, as well as IISc and other institutions (Government labs, Industry and Research Organizations). The facility currently houses more than twenty-five sophisticated instruments for characterization and it operates 24/7 with a dedicated team of about 13 engineers and scientists. The facility is available to all researchers from academia and industry. To know more and to access the characterization equipment in the facility, please visit our website at:

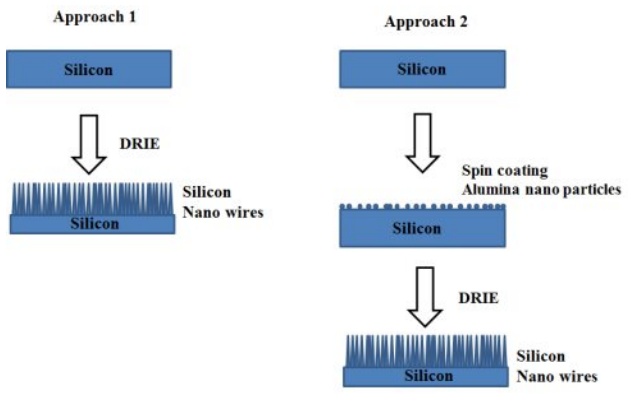
http://www.cense.iisc.ernet.in/mncf/home.htm

Research Highlights: Superhydrophobic Surfaces

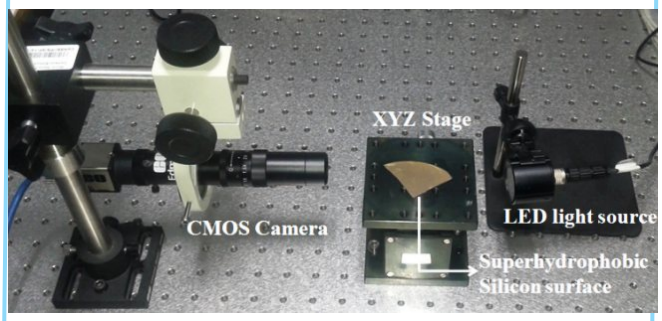
Prosenjit Sen and Abinash Tripathy

Superhydrophobic surfaces show extraordinary water-repellent properties with low drag for fluid flow due to reduced liquid-solid contact area. Due to high contact angle and low contact angle hysteresis, these surfaces also show a self-cleaning effect. In nature, different plants and leaves, such as lotus leaves and rose petals, show superhydrophobic behaviour due to wax-coated micro/nano hierarchical structures on their surfaces. The research work carried out at CeNSE on superhydrophobic surfaces is as follows. Initially, silicon wafers were cleaned by the standard procedure (Piranha, acetone, IPA and water). In the first approach, the wafers were patterned directly by DRIE after the cleaning steps. The high etch selectivity of the DRIE process ensured that micro-masking due to natural variations / contamination on the wafer surface was enough to form nano-structures. In the second approach, a wafer with alumina nano particles on it suspended in ethanol was sonicated to improve dispersion, followed by spin-coating on the silicon substrate. The alumina nanoparticles formed the micro-mask for the etching process. Based on an optimized recipe, DRIE was performed to prepare the nanostructured superhydrophobic surfaces. It is a one-step process and also a large-area fabrication technique.

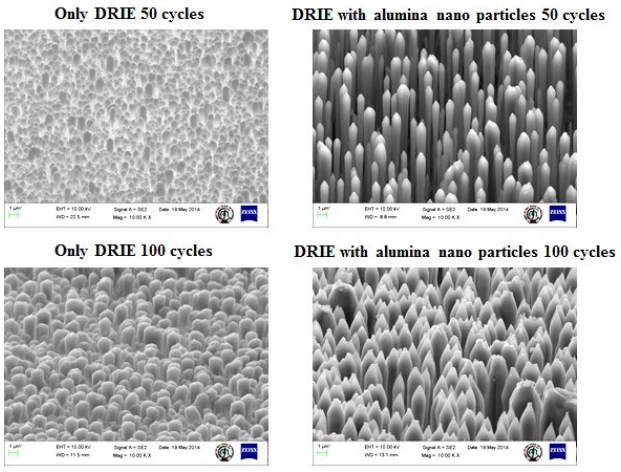
Process Flow for Fabrication



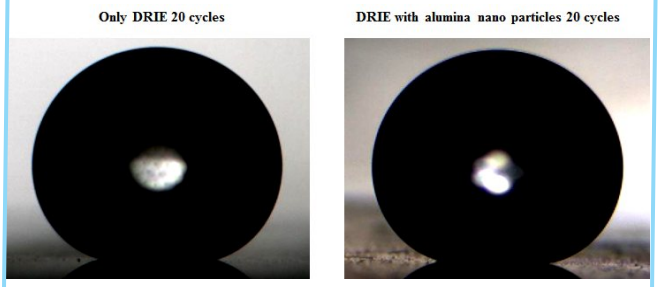
Experimental set up for contact angle measurement



SEM images of nano-structured silicon surface using DRIE



Water droplet on superhydrophobic surface (a) By only DRIE (Contact Angle 168°) (b) By DRIE with alumina nano particles (Contact angle 171°)



CeNSE Updates: Indian Nanoelectronics Users Program (2008- 2014)

S.A. Shivashankar and Sanjeev Srivastava

The Indian Nanoelectronics Users Program (INUP) is a national project initiated in 2008 at IISc-Bangalore and IIT-Bombay by the Department of Electronics and Information Technology (DeitY) of the Govt. of India, and has been the outgrowth of the larger DeitY-funded joint project at the two institutions entitled, "Centre of Excellence in Nanoelectronics" (CEN). Whereas the CEN Project enabled the establishment of the basic infrastructure at the two institutions for fabricating and characterizing nanostructured materials and devices, the INUP was conceived by DeitY as a natural and essential corollary, so that the sophisticated facilities of the CENs could be opened up for use by researchers from various parts of the country – in the academia, public sector R&D centres, and industry.

DeitY was extremely perceptive when the INUP was imagined as a part of the larger CEN initiative, and recognised that merely providing access to the CENs would not be enough, if the funding to do so was also not made available to academic researchers from colleges and universities. Therefore, the policy of the DeitY that made the INUP possible was designed so that such a programme would include funds for providing both training to academic researchers and subsequent access to CEN facilities, on an "all-expenses-paid" basis. Thus, active and aspiring researchers from the smaller institutions in the country would not have to fear that they would be at a disadvantage in obtaining research grants that would be required if they had to meet the costs of using the CENs. INUP provides a platform whereby budding researchers from such institutions gain access to sophisticated laboratories and are mentored by faculty members, senior researchers, and Ph. D. students of the CENs. This is intended to have a multiplier, cascading effect, wherein the faculty members of the participating institutions are encouraged to get involved more intensely in research, to inculcate a healthy research culture among their Ph. D. students, and attempt to build similar capabilities in their own institutions.

Main Objectives of INUP:

a) To provide Nanoelectronics training to researchers from different institutions in India

b) To extend the reach of some aspects of training by organizing awareness workshops at different locations in the country

c) To invite topical and theme-based proposals from researchers time to time, and

d) To encourage and promote projects in which researchers from different institutions collaborate.

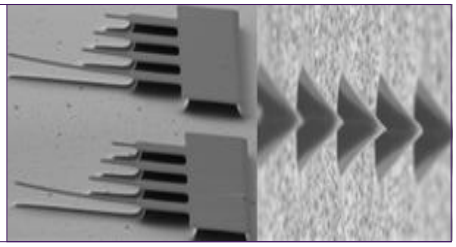
INUP training at IISc:

Level 1: Through three-day Familiarization Workshops held several times a year, researchers are introduced to nanoscience and nano- technology. From among a large number of participants, a smaller number of the most meritorious are selected for an intensive Level 2 training.

Level 2: In the "Hands-on training" Workshops held six times a year (7-10 days each), researchers receive in-the-lab training which enables them to go to Level 3.

Level 3: Extensive training through independent, carefully-vetted research projects at IISc, which often become part of doctoral theses, in addition to generating scholarly publications and intellectual property.

Summary of achievements of INUP at IISc, Bengaluru (2008 - 2013)

Physical Achievements	Target	Achievement (Up to 31st March 2013)	
Familiarization Workshop (Level 1) Manpower trained (Level 1)	5 250	6 563	
Hands-on Training (Level 2) Manpower trained (Level 2)	21 100	22 148	
Research Projects (Level 3) Manpower trained (Level 3)	20 40	85 225	

INUP Event Calendar: October 2014 – March 2015

Hands-on Training	07-16 Oct 2014 9-18 Dec 2014	Completed Completed
Familiarization Workshop	28-30 Jan 2015	Scheduled
Hands-on Training	03-12 Feb 2015 10-19 Mar 2015	Scheduled Scheduled

For more details: http://www.cense.iisc.ernet.in/outreach/inup.htm

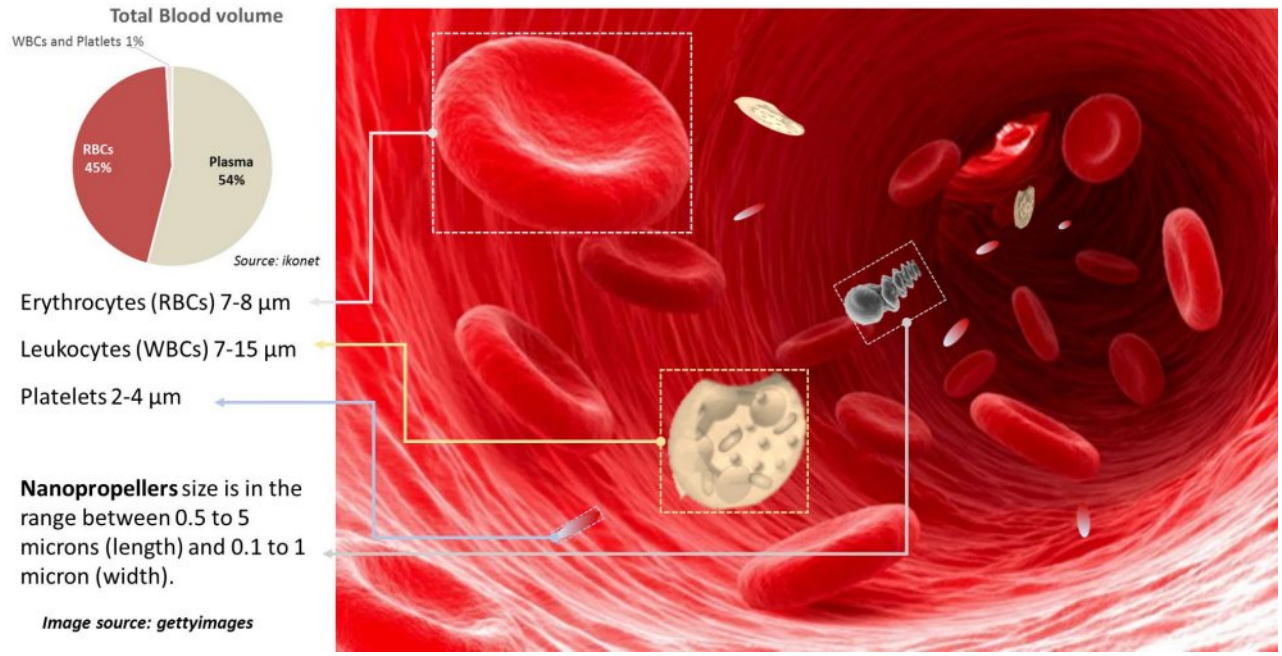
Student Column: Realization of a Nanovoyager in Human Blood

Pooyath Lekshmy Venugopalan

"…it would be interesting in surgery if you could swallow the surgeon. You put the mechanical surgeon inside the blood vessel and it goes into the heart and "looks" around." – Richard Feynman

Given recent advances in nanotechnology, various strategies have been developed to realize this dream of 'nanovoyager', aiming to move artificial nanostructures through harsh biological environments in a controlled manner. As a first demonstration that was recently reported in Nano Letters, magnetic nanohelices were coated conformally with a protective material, thereby leading to the first successful 'voyage' of artificial nanomotor in human blood under in vivo conditions. image The below gives a visual representation of a nanopropeller moving inside a blood vessel. Nanovoyagers reported here were able to move in human blood at the lowest dilution possible with a speed of 15 µm/sec. They were found to be chemically stable in blood even after overnight incubation, owing to the protective ferrite coating. The motion in blood was different from standard Newtonian fluids (such as water) due to the colloidal jamming of blood cells. Standard cytocompatibility methods, such as MTT assay and Fluorescence microscopic analysis of mouse myoblast cells used in this study, confirm the suitability of the ferrite-coated nanopropellers towards possible in vivo applications, such as targeted drug delivery and microsurgery. These ambitious experiments will be attempted in the near future.

Representation of nanopropellers moving inside a blood vessel



Pooyath Lekshmy Venugopalan, Ranajit Sai, Yashoda Chandorkar, Bikramjit Basu, Srinivasrao Shivashankar, and Ambarish Ghosh "Conformal Cytocompatible Ferrite Coatings Facilitate the Realization of a Nanovoyager in Human Blood" Nano Letters 2014, 14, 1968 - 1975.

Alumni Column:

Ranajit Sai, Assistant Professor, Tohoku University, Japan

I belonged to CeNSE even before its first brick had been laid. I was fortunate to witness the formative years of the Centre. The memories from those days are precious and still very fresh. There were more professors and fewer students at that time – during the fresher's welcome of our batch, the second one of the interdisciplinary program 'NI'. However, our journey was not stumble-free. After bumpy coursework, we had to push the available old facilities to the extreme to get our work on track.

Our professors, on the other hand, put immense efforts and showed exemplary commitment to pull something extraordinary out of "shrubs" that stood where CeNSE stands today. Their dedication and enthusiasm inspired us to aim high.

I have been lucky to be a part of such a world-class facility. But, our Centre is far more than mortar and machines. We are blessed with a perfect blend of quality and diversity in our fraternity.

Those varieties of creed, culture, custom, cognition put together form a field fertile enough to germinate and nourish ideas: everything over a cup of coffee. I am missing that atmosphere the most. There is no part of my current professional experience that has not been molded during my stay in CeNSE. I learnt to think critically and coherently. I learnt to question myself and to follow instincts for the answer. I was given ample space and time to appreciate research in my own way. In essence, my time in CeNSE wasn't just the opportunity to meet passionate minds, but the opportunity to witness and participate in the process of creating and sharing knowledge with them. I feel extremely lucky for such incredible experience.

Picture taken by Ranajit Sai of the CeNSE Cleanroom functioning during night hours

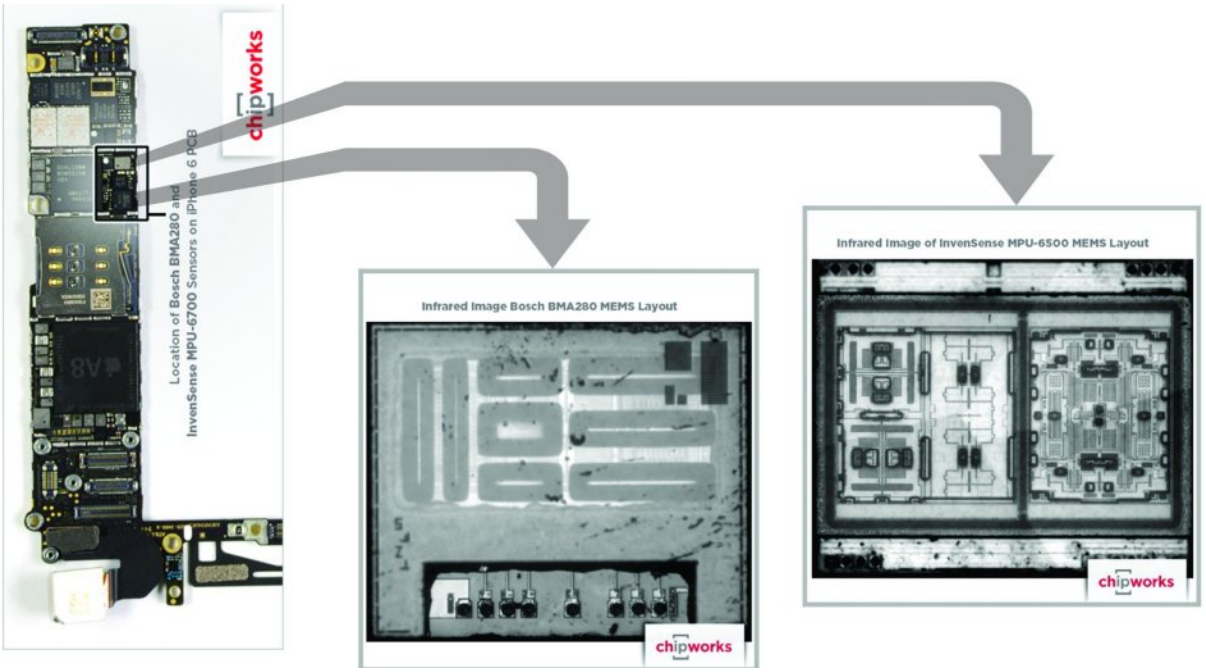
Nanotech Demystified: Accelerometers

Accelerometer technology in Smartphones is demystified (as described by St.J.Dixon-Warren,Chipworks)

The iPhone 6 contains a six-axis InvenSense combination gyroscope-accelerometer and a Bosch BMA280 three-axis accelerometer. There has been some considerable debate in the blogosphere as to why Apple might have incorporated the extra accelerometer functionality. We speculate that the two devices are incorporated to improve the overall user experience, while minimizing power consumption.

The InvenSense device can operate as a sixaxis inertial sensor, or as either a three-axis gyroscope or a three-axis accelerometer. It is rated to consume 3.4 mA in the six-axis mode, 3.2 mA in the gyroscope mode and 450 µA in the accelerometer normal mode. By contrast, the Bosch device operates as a 3 axis accelerometer only and it consumes 130 µA of current in the accelerometer normal mode. Both devices offer two low power levels of operation for the accelerometer function. The InvenSense device actually consumes less current in its lowest power mode, with a 1 Hz update rate. The main benefit of the InvenSense is full six-axis integration of the data by the on-chip digital motion processor (DMP). This will provide a direct benefit for gaming and other applications that need sophisticated inertial sensing capabilities. In addition the InvenSense provides significantly higher sensitivity than the Bosch device. The price however, is higher power consumption. The Bosch device, on the other hand, operates at lowerpower and has a much faster start up. The Bosch device will be used in situations where full six-axis integration is not required and where lower sensitivity is acceptable, for example for purposes such as screen orientation and pedometer functionality. The integration of two accelerometers into the iPhone 6 is another example of Apple's elegant engineering. The phone would have worked with just the InvenSense device, but since not all applications require the higher sensitivity and full six-axis integration, Apple added the Bosch device, which allows them to lower the power consumption while still providing a good user experience.

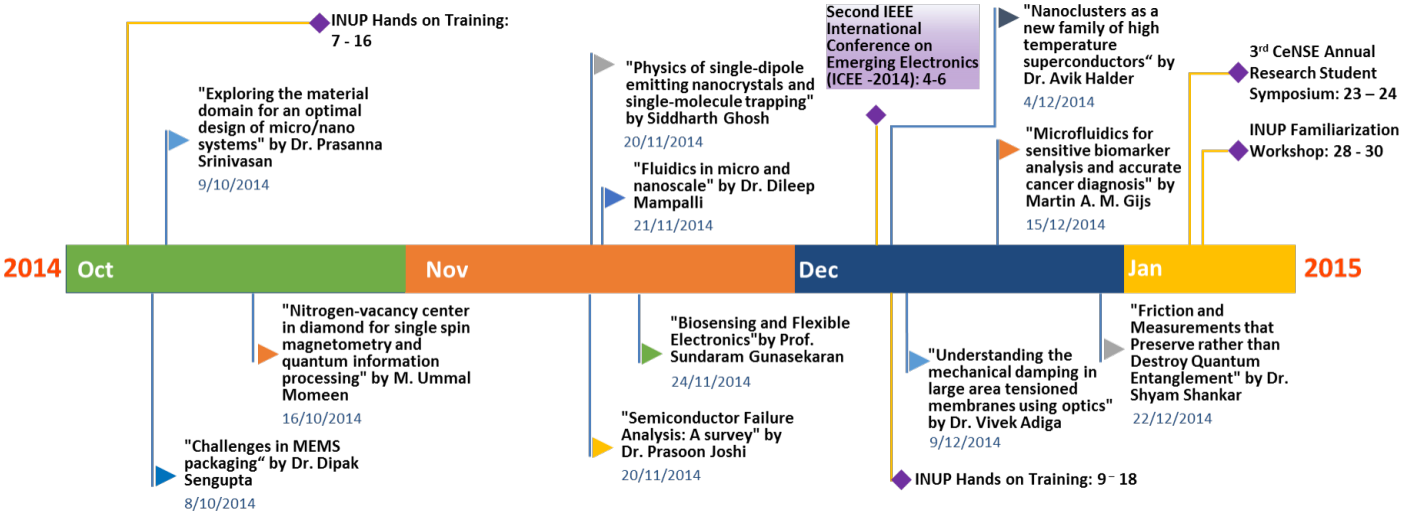
We believe the InvenSense device to be the MPU-6700, based on Chipworks decoding of the package markings. A data sheet is not available for the MPU-6700; however, we expect the specifications to be similar to those published by InvenSense for the MPU-6500. A comparison of the published specs for the BMA280 and the MPU-6500 point to several reasons why Apple might have chosen to include the additional accelerometer functionality.



Source: http://www.chipworks.com/en/technical-competitive-analysis/resources/blog/comparing-the-invensense-and-bosch-accelerometers-found-in-the-iphone-6/ Date: September 2014

Events at CeNSE

The timeline given below shows the events held at CeNSE from October to December 2014 and the upcoming events in January 2015.



Second International Conference on Emerging Electronics (ICEE – 2014)

The second IEEE Conference on Emerging Electronics (ICEE – 2014) was held during December 3-6, 2014 at the J N Tata Auditorium, Indian Institute of Science, Bengaluru. With *Materials to Devices* as the overall theme, the Conference witnessed participation from leading researchers of the world.

The Conference was jointly organised by the IEEE Electron Devices and Solid State Circuits society, Bangalore Chapter and the Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science. Spread over four days, the Conference had eight Plenary Talks and two Public Lectures on a variety of topics ranging from the 'Internet of Things' to Nanoelectronics to using the latest technology to solve quality of life challenges. The galaxy of Plenary Speakers included leading researchers from the Indian Institute of Science, Cornell University (USA), Stanford University (USA), Tata Institute of Fundamental Research (TIFR), and IIT Delhi.

About 500 delegates from different parts of the world presented their research in three parallel sessions. There were also a number of tutorial sessions held on Dec 3 and aimed at students and practitioners alike.

In a series of marathon sessions named *Mind to Market*, people from the academia, manufacturing facilities, and the industries shared their activities and experiences. Industries and startups in the nanotechnology domain expressed appreciation of how they are benefiting from the state-of-the-art facilities available in academic institutions. People from the academia appreciated how their association with the industries has given them a better understanding of the market conditions and customer expectations. The sessions saw participation from people from IITs, IISc, and companies such as Applied Materials and Centum Electronics.

The concluding day of the Conference saw an engaging panel discussion on Emergence of India as an Electronics Powerhouse. The august panel consisted of people from the Government of India, industry and academia. The Conference was sponsored by the Office of Naval Research, USA, CSIR, DRDO, Department of Electronics and Information Technology, Department of Science and Technology, and Aeronautical Development Agency, and many other private and government organisations.

Compiled by Science Media Center, IISc.

Glimpses of ICEE - 2014

Inaugural address by Prof. Rudra Pratap, Chairman CeNSE IISc

Plenary talk on the Internet of Things by Prof. Anurag Kumar, Director IISc

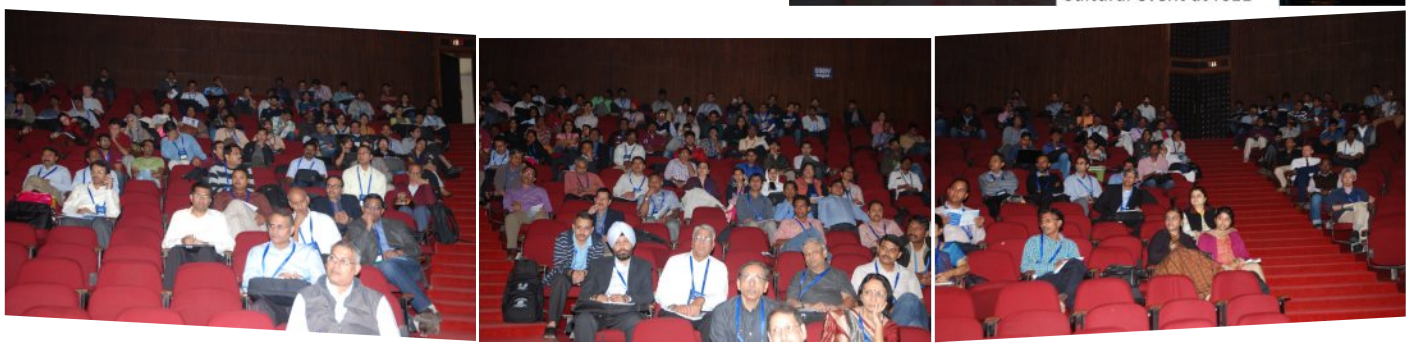
Technical talks

Mind to Market sessions

Panel Discussion: Emergence of India as Electronics Powerhouse

Group photo of ICEE CeNSE team

Cultural event at ICEE



CeNSE Visitors

Dr. Arvind Gupta, Deputy National Security Advisor, GoI, visited CeNSE IISc on 25th September 2014 -

"It was an honour and to visit the Centre and be educated on the Nano Science and Technology work being done here. The facility here is great and doing that which helps in building the nation and its capabilities. Congratulations and best of luck!"

Dr. Lalji Singh, Former Director CCMB and former Vice Chancellor of Banaras Hindu University, Varanasi ,visited CeNSE IISc on 26th September 2014,

"CeNSE Facilities are outstanding. I'm overwhelmed to see this facility built, organized and equipped well. I see my dream fulfilled. I am proud of it and I'm sure our country will be proud of its performance in future. I wish all scientists working here success"

Awards Column

DRDO's Academic Excellence Award is given to academicians associated with DRDO for research in emerging areas. The Prime Minister, **Shri Narendra Modi** presented the Academic Excellence Award 2013 to **Emeritus Prof. S. Mohan** at the DRDO Awards presentation ceremony, in New Delhi on August 20, 2014, for his noteworthy contributions to several projects of DRDO.

Also seen are ***Shri Arun Jaitley,*** *Union Minister for Finance, Corporate Affairs and Defence,*

Shri Rao Inderjit Singh*, Minister of State for planning (independent charge), Statistics and Programme Implementation, and*

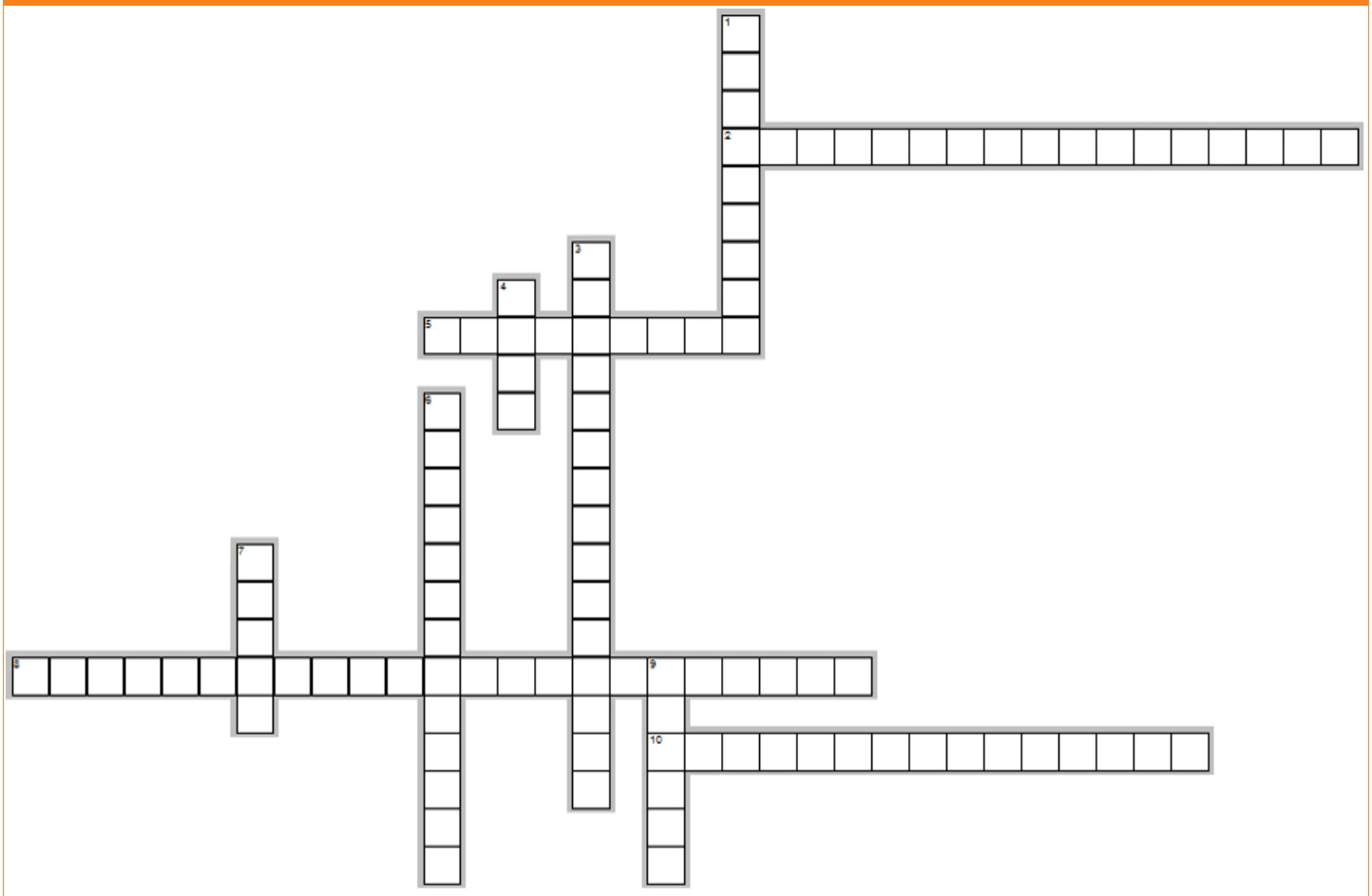
Shri Avinash Chander*, Secretary, Department of Defence R&D, DG R&D and SA to RM.*

"Prof. Ramakrishna Rao Chair Professorships" endowed by Centum Electronics are now held by

Prof. Srinivasan Raghavan (Vasu), CeNSE

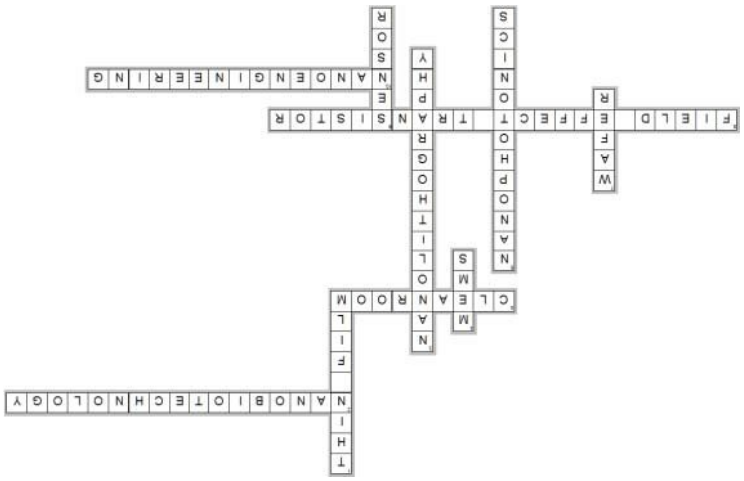
Prof. Jeevak M. Parpia, Cornell University

Nanocrossword



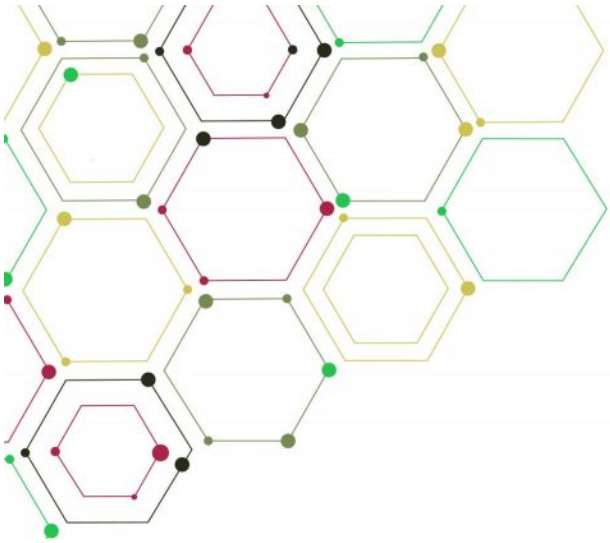
Across

2. This discipline that helps to indicate the merger of biological research with various fields of nanotechnology.
5. An environment free from dust and other contaminants, used chiefly for the manufacture of electronic components.
8. A transistor that uses an electric field to control the shape and hence the conductivity of a channel of one type of charge carrier in a semiconductor material.
10. Practice of engineering on the nanoscale



Down

1. A layer of material ranging from fractions of a nanometer (monolayer) to several micrometers in thickness.
3. The art and science of etching, writing, or printing at the microscopic level, where the dimensions of characters are on the order of nanometers (units of 10-9 meter, or millionths of a millimeter).
4. It is a technology of very small devices
6. The study of the behaviour of light on the nanometer scale, and of the interaction of nanometer-scale objects with light.
7. It is also called a slice or substrate, and is a thin slice of semiconductor material
9. A device that detects events or changes in quantities and provides a corresponding output, generally as an electrical or optical signal.



CeNSE Newsletter is published by the Centre for Nano Science and Engineering to keep the community of academia, industry, and government organizations informed of the activities and accomplishments of the Centre.

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